

MUFFAKHAM JAH
COLLEGE OF ENGINEERING AND TECHNOLOGY

EC-241 ELECTRONIC ENGINEERING - 1 LAB

(For EEE & EIE)

(With effect from the academic year 2015-2016)

STUDENT'S MANUAL



**DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING**

Vision and Mission of the Institution

Vision

To be part of universal human quest for development and progress by contributing high calibre, ethical and socially responsible engineers who meet the global challenge of building modern society in harmony with nature.

Mission

- To attain excellence in imparting technical education from the undergraduate through doctorate levels by adopting coherent and judiciously coordinated curricular and co-curricular programs
- To foster partnership with industry and government agencies through collaborative research and consultancy
- To nurture and strengthen auxiliary soft skills for overall development and improved employability in a multi-cultural work space
- To develop scientific temper and spirit of enquiry in order to harness the latent innovative talents
- To develop constructive attitude in students towards the task of nation building and empower them to become future leaders
- To nourish the entrepreneurial instincts of the students and hone their business acumen.
- To involve the students and the faculty in solving local community problems through economical and sustainable solutions.

Vision and Mission of ECE Department

Vision

To be recognized as a premier education center providing state of art education and facilitating research and innovation in the field of Electronics and Communication.

Mission

We are dedicated to providing high quality, holistic education in Electronics and Communication Engineering that prepares the students for successful pursuit of higher education and challenging careers in research, R& D and Academics.

Program Educational Objectives of B. E (ECE) Program:

1. Graduates will demonstrate technical competence in their chosen fields of employment by identifying, formulating, analyzing and providing engineering solutions using current techniques and tools
2. Graduates will communicate effectively as individuals or team members and demonstrate leadership skills to be successful in the local and global cross-cultural working environment
3. Graduates will demonstrate lifelong learning through continuing education and professional development
4. Graduates will be successful in providing viable and sustainable solutions within societal, professional, environmental and ethical contexts

MUFFAKHAM JAH COLLEGE OF ENGINEERING AND TECHNOLOGY
BANJARA HILLS, ROAD NO-3, TELANGANA



LABORATORY MANUAL
FOR
ELECTRONIC ENGINEERING –I LAB

Prepared by:

Checked by:

Approved by:

MUFFAKHAM JAH COLLEGE OF ENGINEERING AND TECHNOLOGY**DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING****(Name of the Subject/Lab Course): Electronic Engineering –I lab****Code: EC241****Programme: UG****Branch: ECE****Version No: 1****Year : II****Updated on: 20/3/16****Semester :I****No. of Pages:****Classification Status(Unrestricted/restricted): Unrestricted****Distribution List :Department, Lab, Library, Lab Incharge****Prepared by: 1) Name :****1) Name :****2) Sign :****2) Sign :****3)Designation :****3) Designation :****4) Date :****4) Date :****Verified by: 1) Name :***** For Q.C Only****2) Sign :****1) Name :****3)Designation :****2) Sign :****4) Date :****3) Designation :****4) Date :****Approved by: (HOD) 1) Name:****2) Sign :****3) Date :**

ELECTRONIC ENGINEERING-I LAB

Instruction	3 Periods per Week
Duration of University Examination	3Hours
University Examination	50Marks
Sessional	25Marks

Objectives:

1. Obtain V-I Characteristics of PN, Zener diodes, Tunnel and photo diodes, UJT, SCR, BJT and JFET.
2. Design rectifier circuits with and without capacitor filters.
3. Explain the working principle of CRO.

INDEX

1. V-I Characteristics of Silicon and Germanium diodes.
2. Zener diode Characteristics and its application as regulator
3. Half Wave and Full wave rectifier without filter
4. Half Wave and Full wave rectifier with filter
5. Characteristics of BJT in Common Emitter configuration
6. JFET Characteristics
7. Study of CRO and its Application
8. BJT Biasing Circuits
9. Common Emitter BJT Amplifier
10. Common Source JFET Amplifier
11. Characteristics of UJT and SCR

ELECTRONIC ENGINEERING-I LAB

GENERAL GUIDELINES AND SAFETY INSTRUCTIONS

1. Sign in the log register as soon as you enter the lab and strictly observe your lab timings.
2. Strictly follow the written and verbal instructions given by the teacher / Lab Instructor. If you do not understand the instructions, the handouts and the procedures, ask the instructor or teacher.
3. **Never work alone!** You should be accompanied by your laboratory partner and / or the instructors / teaching assistants all the time.
4. It is mandatory to come to lab in a formal dress and wear your ID cards.
5. Do not wear loose-fitting clothing or jewellery in the lab. Rings and necklaces are usual excellent conductors of electricity.
6. Mobile phones should be switched off in the lab. Keep bags in the bag rack.
7. Keep the labs clean at all times, no food and drinks allowed inside the lab.
8. Intentional misconduct will lead to expulsion from the lab.
9. Do not handle any equipment without reading the safety instructions. Read the handout and procedures in the Lab Manual before starting the experiments.
10. Do your wiring, setup, and a careful circuit checkout before applying power. Do not make circuit changes or perform any wiring when power is on.
11. Avoid contact with energized electrical circuits.
12. Do not insert connectors forcefully into the sockets.
13. **NEVER** try to experiment with the power from the wall plug.
14. Immediately report dangerous or exceptional conditions to the Lab instructor / teacher: Equipment that is not working as expected, wires or connectors are broken, the equipment that smells or “smokes”. If you are not sure what the problem is or what's going on, switch off the Emergency shutdown.
15. Never use damaged instruments, wires or connectors. Hand over these parts to the Lab instructor/Teacher.
16. Be sure of location of fire extinguishers and first aid kits in the laboratory.
17. After completion of Experiment, return the bread board, trainer kits, wires, CRO probes and other components to lab staff. Do not take any item from the lab without permission.
18. Observation book and lab record should be carried to each lab. Readings of current lab experiment are to be entered in Observation book and previous lab experiment should be written in Lab record book. Both the books should be corrected by the faculty in each lab.
19. Handling of Semiconductor Components: Sensitive electronic circuits and electronic components have to be handled with great care. The inappropriate handling of electronic component can damage or destroy the devices. The devices can be destroyed by driving to high currents through the device, by overheating the device, by mixing up the polarity, or by electrostatic discharge (ESD). Therefore, always handle the electronic devices as indicated by the handout, the specifications in the data sheet or other documentation.
20. Special Precautions during soldering practice
 - a. Hold the soldering iron away from your body. Don't point the iron towards you.
 - b. Don't use a spread solder on the board as it may cause short circuit.
 - c. Do not overheat the components as excess heat may damage the components/board.
 - d. In case of burn or injury seek first aid available in the lab or at the college dispensary

List of Experiments	Page
1. V-I Characteristics of Silicon and Germanium diodes.	8
2. Zener diode Characteristics and its application as regulator	14
3. Half Wave and Full wave rectifier without filter	20
4. Half Wave and Full wave rectifier with filter	27
5. Characteristics of BJT in Common Emitter configuration	32
6. JFET Characteristics	38
7. Study of CRO and its Application	42
8. BJT Biasing Circuits	49
9. Common Emitter BJT Amplifier	53
10. Common Source JFET Amplifier	57
11. Characteristics of UJT and SCR	61
12. Appendix	68

Experiment No:1

P - N Junction Diode Characteristics

Aim:

1. To plot Volt-Ampere Characteristics of Silicon and Germanium P-N Diode.
2. To find cut-in voltage for Silicon and Germanium P-N Junction diode.
3. To find static and dynamic resistances in both forward and reverse biased conditions.

Components:

Name	Quantity
Diodes 1N4007(Si)	1
Diodes DR-25(Ge)	1
Resistor 1K Ω	1
Resistor 3.3K Ω	1

Equipment:

Name	Range	Quantity
Bread board		1
Regulated power supply	0-30V	1
Digital Ammeter	0-200 μ A/200mA	1
Digital Voltmeter	0-20V	1
Connecting Wires		

Specifications:**Silicon Diode 1N4007:**

Max Forward Current = 1A
 Max Reverse Current = 5.0 μ A
 Max Forward Voltage = 0.8V
 Max Reverse Voltage = 1000V
 Max Power Dissipation = 30mW
 Temperature = -65 to 200° C

Germanium Diode DR-25:

Max Forward Current = 250mA
 Max Reverse Current = 200 μ A
 Max Forward Voltage = 1V
 Max Reverse Voltage = 25V
 Max Power Dissipation = 250mW
 Temperature = -55 to 75° C

Theory:

Donor impurities (pentavalent) are introduced into one-side and acceptor impurities into the other side of a single crystal of an intrinsic semiconductor to form a p-n diode with a junction called depletion region (this region is depleted of the charge carriers). This region gives rise to a potential barrier called Cut-in Voltage. This is the voltage across the diode at which it starts conducting. The P-N junction can conduct beyond this potential.

The P-N junction supports uni-directional current flow. If +ve terminal of the input supply is connected to anode (P-side) and -ve terminal of the input supply is connected to the cathode. Then diode is said to be forward biased. In this condition the height of the potential barrier at the junction is lowered by an amount equal to given forward biasing voltage. Both the holes

from p-side and electrons from n-side cross the junction simultaneously and constitute a forward current from n-side (injected minority current – due to holes crossing the junction and entering P- side of the diode). Assuming current flowing through the diode to be very large, the diode can be approximated as short- circuited switch.

If –ve terminal of the input supply is connected to anode (p-side) and +ve terminal of the input supply is connected to cathode (n-side) then the diode is said to be reverse biased. In this condition an amount equal to reverse biasing voltage increases the height of the potential barrier at the junction. Both the holes on P-side and electrons on N-side tend to move away from the junction there by increasing the depleted region. However the process cannot continue indefinitely, thus a small current called reverse saturation current continues to flow in the diode. This current is due to be negligible; the diode can be approximated as an open circuited switch.

The volt-ampere characteristics of a diode explained by the following equations:

$$I = I_0 \left(e^{\frac{V_D}{\eta V_T}} - 1 \right)$$

Where ,I = current flowing in the diode, I_0 = reverse saturation current

V_D = Voltage applied to the diode

V_T = volt- equivalent of temperature = $k T/q = T/ 11,600 = 26\text{mV}$ (@ room temp)

$\eta = 1$ (for Ge) and 2 (for Si)

It is observed that **Ge** diodes has smaller cut-in-voltage when compared to **Si** diode. The reverse saturation current in **Ge** diode is larger in magnitude when compared to silicon diode.

Theoretically the dynamic resistance of a diode is determined using the following equation:

Dynamic Resistance:

$$R_D = \frac{\eta V_T}{I}$$

Circuit Diagrams:

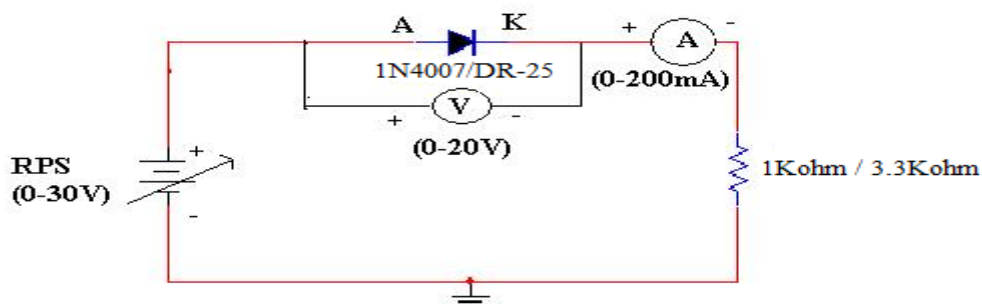


Fig. (1) - Forward Bias Condition

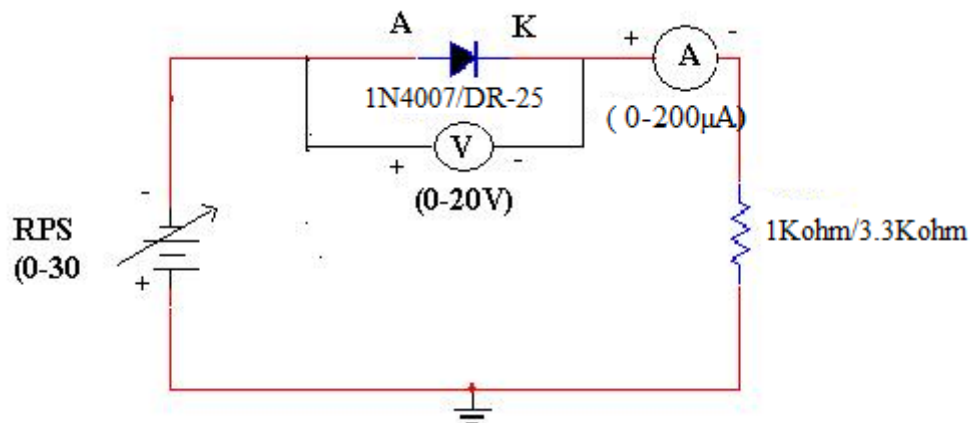


Fig. (2) - Reverse Bias Condition

Procedure:**Forward Bias Condition:**

1. Connect the components as shown in the circuit diagram (1).
2. Vary the supply voltage such that the voltage across the Silicon diode varies from 0 to 0.6 V in steps of 0.1 V and in steps of 0.02 V from 0.6 to 0.76 V. In each step record the current flowing through the diode as I.
3. Repeat the above steps for Germanium diode too but with the exception that the voltage across the diode should be varied in steps of 0.01 V from 0.1 to 0.3 V in step-2.

Reverse Bias Condition:

1. Connect the diode in the reverse bias as shown in the circuit diagram (2)
2. Vary the supply voltage such that the voltage across the diode varies from 0 to 10V in steps of 1 V. Record the current flowing through the diode in each step.
3. Repeat the above steps for Germanium diode too and record the current in each step.
4. Now plot a graph between the voltage across the diode and the current flowing through the diode in forward and reverse bias, for Silicon and Germanium diodes on separate graph sheets. This graph is called the V-I characteristics of the diode.
5. Calculate the static and dynamic resistance of each diode in forward and reverse bias using the following formulae.

$$\text{Static resistance, } R = V/I$$

$$\text{Dynamic resistance, } r = \Delta V/\Delta I$$

Observations:

(a) Forward and Reverse bias characteristics of Silicon diode

Forward Bias Condition:

S. No.	Forward Voltage across the diode (volts) V_d (Volt)	Forward Current through the diode I_d (mA)

Reverse Bias Condition:

S. No.	Reverse Voltage across the diode (volts) V_r (Volt)	Reverse Current through the diode I_d (μA)

Forward and Reverse bias characteristics of Germanium diode

Forward Bias Condition:

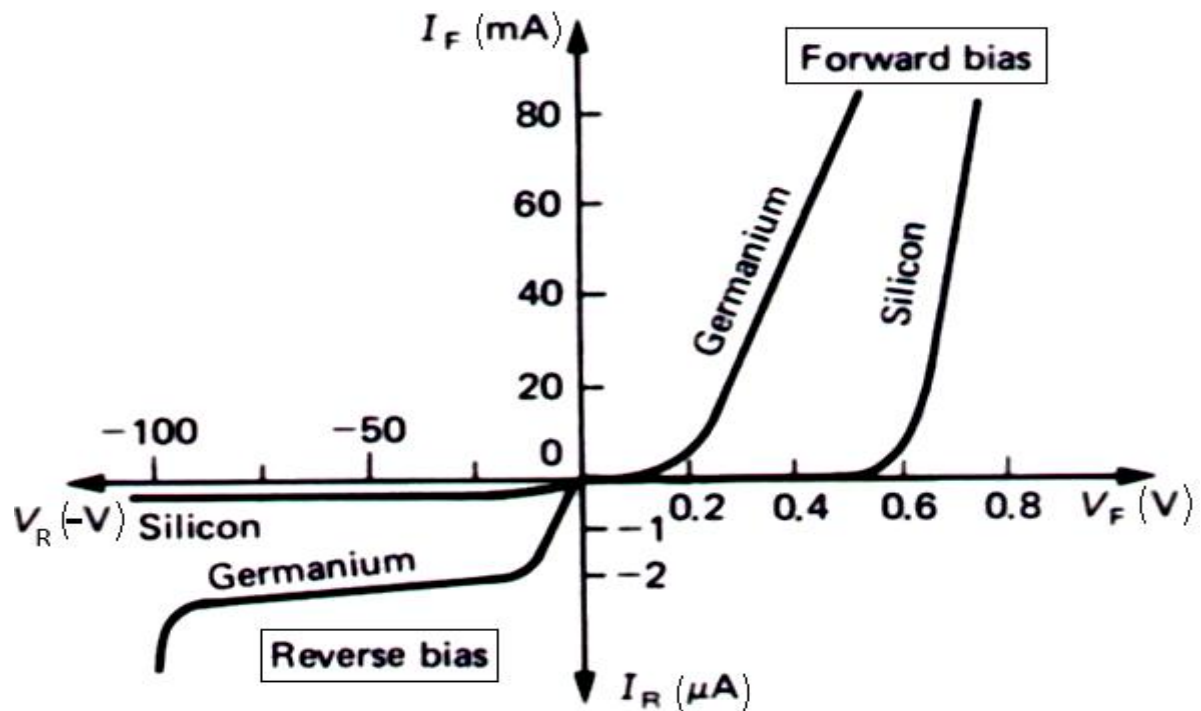
S. No.	Forward Voltage across the diode (volts) V_d (Volt)	Forward Current through the diode I_d (mA)

Reverse Bias Condition:

S. No.	Reverse Voltage across the diode (volts) V_r (Volt)	Reverse Current through the diode I_d (μA)

Graph:

1. Take a graph sheet and divide it into 4 equal parts. Mark origin at the center of the graph sheet.
2. Now mark +ve X-axis as , -ve X-axis as , +ve Y-axis as and -ve Y-axis as .
3. Mark the readings tabulated for Si forward biased condition in first Quadrant and Si reverse biased condition in third Quadrant.
4. Repeat the same procedure for plotting the Germanium characteristics.

**Calculations from Graph:**

Static forward Resistance

$$R_{dc} = V_f / I_f \Omega$$

Dynamic Forward Resistance

$$r_{ac} = \Delta V_f / \Delta I_f \Omega$$

Static Reverse Resistance

$$R_{dc} = V_r / I_r \Omega$$

Dynamic Reverse Resistance

$$r_{ac} = \Delta V_r / \Delta I_r \Omega$$

Precautions:

1. While doing the experiment do not exceed the readings of the diode. This may lead to damaging of the diode.
2. Connect voltmeter and ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

Result:

Cut in voltage = _____ V

Static Forward Resistance = _____ Ω Dynamic Forward Resistance = _____ Ω Static Reverse Resistance = _____ Ω Dynamic Reverse Resistance = _____ Ω

Volt-Ampere Characteristics of Silicon P-N Diode are studied.

Viva Questions:**1. What are trivalent and pentavalent impurities?**

Ans: Doping is the process of adding impurity atoms to intrinsic silicon or germanium to improve the conductivity of the semiconductor.

Commonly Used Doping Elements

Trivalent Impurities to make p-Type: Aluminum (Al), Gallium (Ga), Boron(B) and Indium (In).

Pentavalent Impurities to make n-type: Phosphorus (P), Arsenic (As), Antimony (Sb) and Bismuth (Bi).

2. How PN junction diode does acts as a switch?

Ans: Apply voltage in one direction; it acts like an open circuit. Reverse the polarity of the voltage and it acts like a short circuit.

3. Diode current equation?

Ans: $I = I_S(e^{V_D/(\eta V_T)} - 1)$

4. What is the value of V_t at room temperature?

Ans: 25mV

5. Dynamic resistance expression?

Ans: $r_d = \Delta V / \Delta I$

Experiment No.:2

Zener Diode Characteristics

Aim:

1. To plot Volt-Ampere Characteristics of Zener Diode.
2. To find Zener break down voltage in reverse biased conditions.
3. To study the operation of Zener Diode as a voltage shunt regulator.

Components:

Name	Quantity
Zener Diodes 1N4735A	1
Resistor 1K Ω	1

Equipments:

Name	Range	Quantity
Bread board		1
Regulated power supply	0-30V	1
Digital Ammeter	200mA	1
Digital Voltmeter	0-20V	1
Connecting Wires		

Specifications:

- Breakdown Voltage = 5.1V
- Power dissipation = 0.75W
- Max Forward Current = 1A

Theory:

An ideal P-N junction diode does not conduct in reverse biased condition. A Zener diode conducts excellently even in reverse biased condition. These diodes operate at a precise value of voltage called break down voltage. It is normally a heavily doped Silicon diode.

A Zener diode when forward biased behaves like an ordinary P-N junction diode.

A Zener diode when reverse biased can undergo avalanche break down or zener break down.

Avalanche Break down:

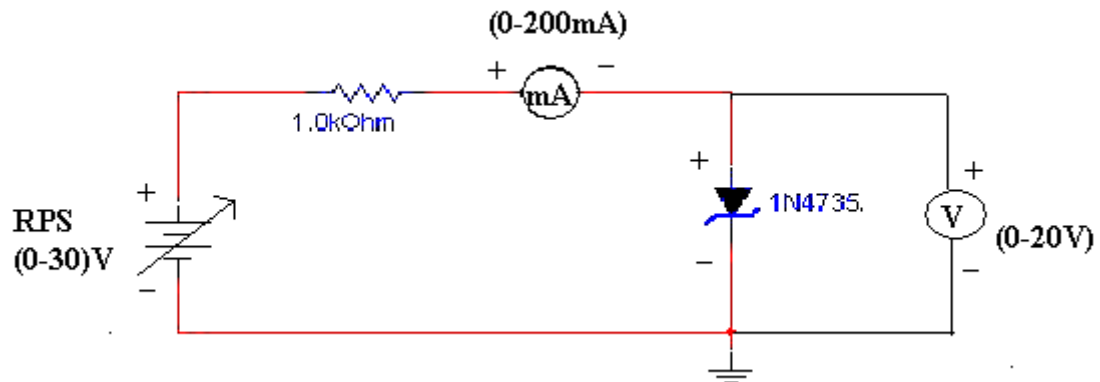
If both p-side and n-side of the diode are lightly doped, depletion region at the junction widens. Application of a very large electric field at the junction may rupture covalent bonding between electrons. Such rupture leads to the generation of a large number of charge carriers resulting in Avalanche Breakdown.

Zener Break down:

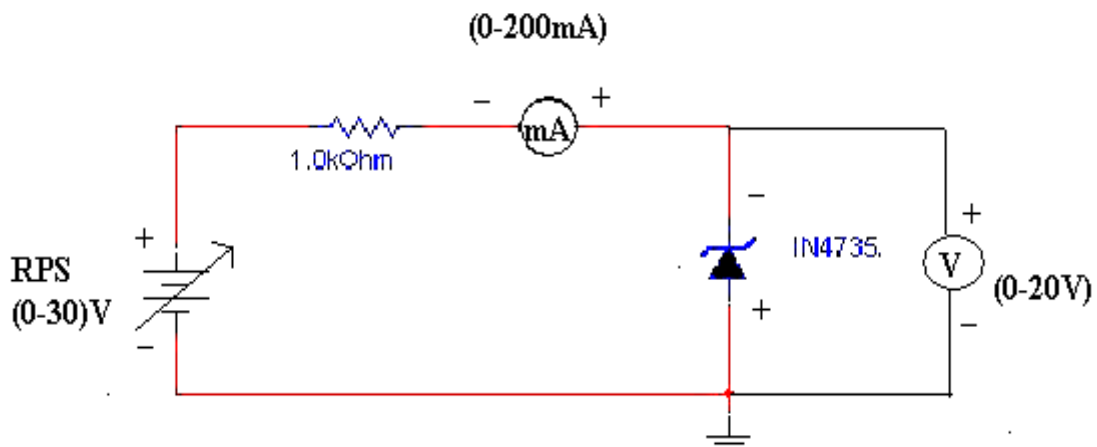
If both p-side and n-side of the diode are heavily doped, depletion region at the junction reduces. Application of even a small voltage at the junction may rupture covalent bonding and generate large number of charge carriers. Such sudden increase in the number of charge carriers results in zener mechanism.

Regulator is an electronic circuit that can provide a stable DC voltage irrespective of variations in the supply voltage, load current and temperature. A Zener diode can be used as a regulator.

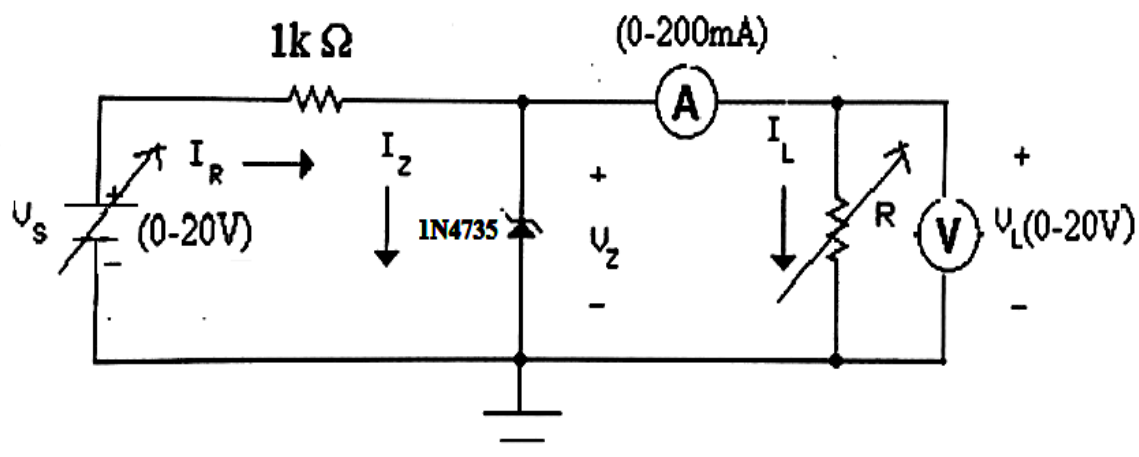
Circuit Diagram:



Fig(1)- Forward Bias Condition:



Fig(2)- Reverse Bias Condition:



Fig(3)- Line Regulation and Load Regulation

Procedure:**Forward Bias Condition:**

1. Connect the circuit as shown in figure (1).
2. Vary V_{zf} gradually and note down the corresponding readings of I_{zf} .
3. Step size is not fixed because of non-linear curve and varies the X- axis variable (i.e., if output variation is more, decrease input step size and vice versa).
4. Tabulate different forward currents obtained for different forward voltages.

Reverse Bias Condition:

1. Connect the circuit as shown in figure (2).
2. Vary V_{zr} gradually and note down the corresponding readings of I_{zr} .
3. Step size is not fixed because of non-linear curve and varies the X- axis variable (i.e., if output variation is more, decrease input step size and vice versa).
4. Tabulate different reverse currents obtained for different reverse voltages.

Line regulation Characteristics:

- 1) Connect the circuit as shown in figure-3.
- 2) Keep the Load Resistance Constant at $10k\Omega$.
- 3) Vary the supply voltage V_s in steps of 1volt starting from 0 volt to 15 volt and note the corresponding value of load voltage (V_L).
- 4) Plot a graph between the supply voltage V_s and the output voltage V_L . This graph is called the line regulation characteristics.

Load regulation characteristics:

- 1) Connect the circuit as shown in figure-3. Use a Decade Resistance Box (DRB) in place of the load.
- 2) Set the supply voltage to 12 V and adjust the load current to 0 mA by keeping the resistance in the DRB at its maximum value.
- 3) Vary load resistance such that the load current (I_L) is increased in steps of 1 mA from 0 mA to 10 mA and note the voltage at the output (V_o). The supply voltage must be maintained constant at 12 V throughout the experiment in part-iii.
- 4) Plot a graph between the load current I_L and the output voltage V_o . This graph is called the load regulation characteristics.

Observations:**Forward Bias Condition:**

S.No.	Forward Voltage across the diode V_{zf} (volts)	Forward Current through the diode I_{zf} (mA)

Reverse Bias Condition:

S.No.	Reverse Voltage across the diode V_{zr} (volts)	Reverse Current through the diode I_{zr} (mA)

b) Line regulation characteristics:

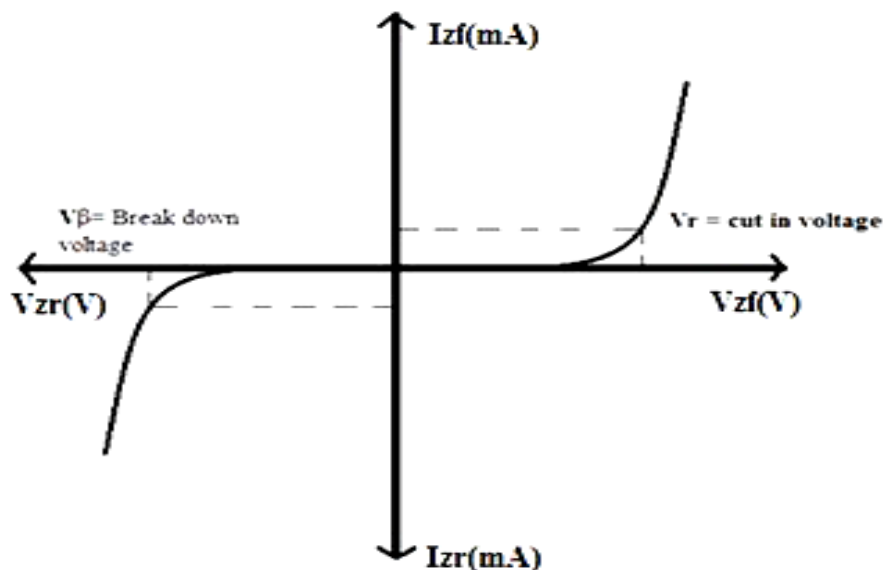
S. No.	V_s (Volt)	V_L (volt)

c) Load regulation characteristics:

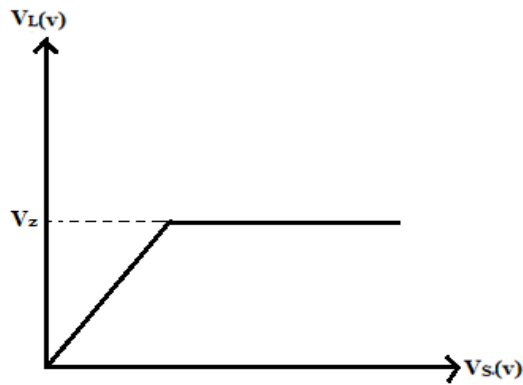
S. No.	I_L (mA)	V_L (volt)

Graph:

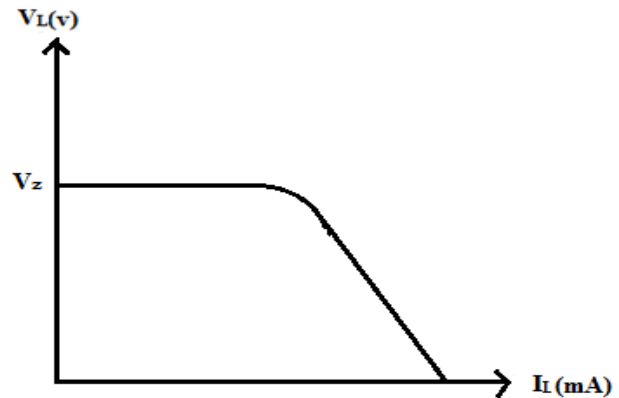
1. Take a graph sheet and divide it into 4 equal parts. Mark origin at the center of the graph sheet.
2. Now mark +ve X-axis as V_{zf} , -ve X-axis as V_{zr} , +ve Y-axis as I_{zf} and -ve Y-axis as I_{zr} .
3. Mark the readings tabulated for forward biased condition in first Quadrant and reverse biased condition in third Quadrant.



Fig(4).VI Characteristics of Zener Diode



Fig(5). Line Regulation



Fig(6). Load Regulation

Calculations from Graph:**Precautions:**

1. While doing the experiment do not exceed the readings of the diode. This may lead to damaging of the diode.
2. Connect voltmeter and ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

Result:

1. The Zener Diode Characteristics have been studied.
2. The breakdown voltage of Zener diode in reverse bias was found to be = _____
3. Zener Diode as a shunt voltage regulator is studied.

Viva Questions:**1. What is the difference between p-n Junction diode and zener diode?**

Ans: A zener is designed to operate stably in reverse breakdown, which is designed to be at a low voltage, between 3 volts and 200 volts. The breakdown voltage is specified as a voltage with a tolerance, such as 10 volts $\pm 5\%$, which means the breakdown voltage (or operating voltage) will be between 9.5 volts and 10.5 volts. A signal diode or rectifier will have a high reverse breakdown, from 50 to 2000 volts, and is NOT designed to operate in the breakdown region. So exceeding the reverse voltage may result in the device being damaged. In addition, the breakdown voltage is specified as a minimum only.

Forward characteristics are similar to both, although the zener's forward characteristics is usually not specified, as the zener will never be used in that region. A signal diode or rectifier has the forward voltage specified as a max voltage at one or more current levels.

2. What is break down voltage?

Ans: The breakdown voltage of a **diode** is the minimum reverse voltage to make the diode conduct in reverse.

3. What are the applications of Zener diode?

Ans: Zener diodes are widely used as voltage references and as **shunt regulators** to regulate the voltage across small circuits.

4. What is cut-in-voltage ?

Ans: The forward voltage at which the current through the junction starts increasing rapidly, is called the knee voltage or cut-in voltage. It is generally 0.6v for a Silicon diode.

5. What is voltage regulator?

Ans: A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature and ac line voltage variations

Experiment No:3**Half Wave and Full Wave Rectifier Without Filter****Aim:** (i) To study the operation of Half wave and Full wave rectifier without filter

(ii) To find its:

1. Ripple Factor
2. Efficiency
3. Percentage Regulation

Components:

Name	Quantity
Diodes 1N4007(Si)	2
Resistor 1K Ω	1

Equipment:

Name	Range	Quantity
CRO	0-1MHz	1
CRO probes	----	2
Multimeter	----	1
Transformer	220V/9V, 50Hz	1
Connecting Wires	----	----

Specifications:**Silicon Diode 1N4007:**

Max Forward Current = 1A

Max Reverse Current = 5.0 μ A

Max Forward Voltage = 0.8V

Max Reverse Voltage = 1000V

Max Power Dissipation = 30mW

Temperature = -65 to 200° C

Theory:

A rectifier is a circuit that converts a pure AC signal into a pulsating DC signal or a signal that is a combination of AC and DC components.

A half wave rectifier makes use of single diode to carry out this conversion. It is named so as the conversion occurs for half input signal cycle.

During the positive half cycle, the diode is forward biased and it conducts and hence a current flows through the load resistor.

During the negative half cycle, the diode is reverse biased and it is equivalent to an open circuit, hence the current through the load resistance is zero. Thus the diode conducts only for one half cycle and results in a half wave rectified output.

A full wave rectifier makes use of a two diodes to carry out this conversion. It is named so as the conversion occurs for complete input signal cycle.

The full-wave rectifier consists of a center-tap transformer, which results in equal voltages above and below the center-tap. During the positive half cycle, a positive voltage appears at the anode of D1 while a negative voltage appears at the anode of D2. Due to this diode D1 is forward biased it results in a current I_{d1} through the load R.

During the negative half cycle, a positive voltage appears at the anode of D2 and hence it is forward biased. Resulting in a current I_{d2} through the load at the same instant a negative voltage appears at the anode of D1 thus reverse biasing it and hence it doesn't conduct.

Ripple Factor:

Ripple factor is defined as the ratio of the effective value of AC components to the average DC value. It is denoted by the symbol ' γ '.

$$\gamma_{HWR} = \frac{V_{AC}}{V_{DC}} = 1.21$$

$$\gamma_{FWR} = \frac{V_{AC}}{V_{DC}} = 0.48$$

Rectification Factor:

The ratio of output DC power to input AC power is defined as efficiency.

$$\eta = \frac{(V_{DC})^2}{(V_{AC})^2}$$

$$\eta_{HWR} = 40.6\%$$

$$\eta_{FWR} = 81\%$$

Percentage of Regulation:

It is a measure of the variation of AC output voltage as a function of DC output voltage.

$$\text{Percentage of regulation} = \left(\frac{V_{NL} - V_{FL}}{V_{FL}} \right) * 100 \%$$

V_{NL} = Voltage across load resistance, when minimum current flows through it.

V_{FL} = Voltage across load resistance, when maximum current flows through.

For an ideal rectifier, the percentage regulation is 0 percent. The percentage of regulation is very small for a practical half wave and full wave rectifier.

Peak- Inverse – Voltage (PIV):

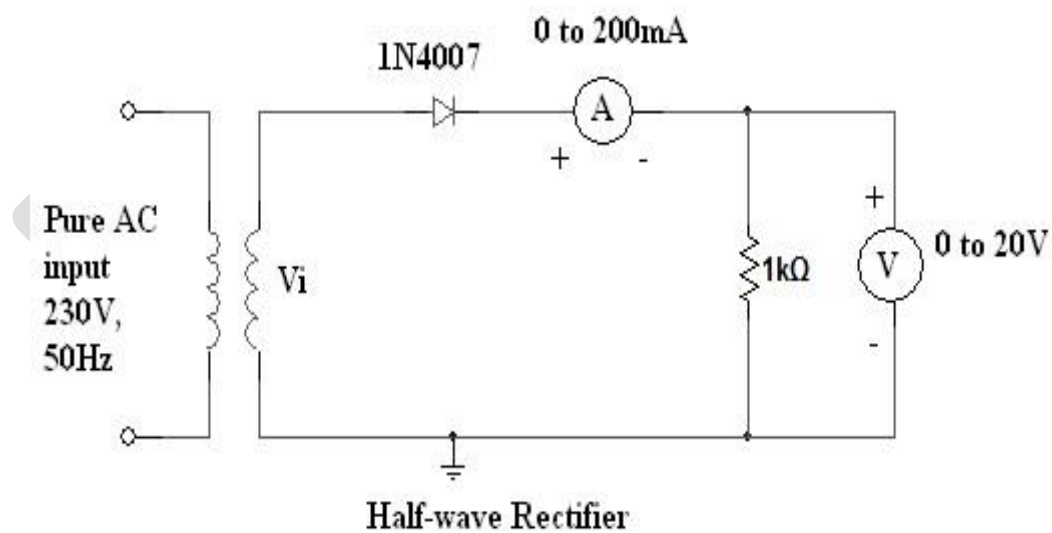
It is the maximum voltage that has to be with stood by a diode when it is reverse biased

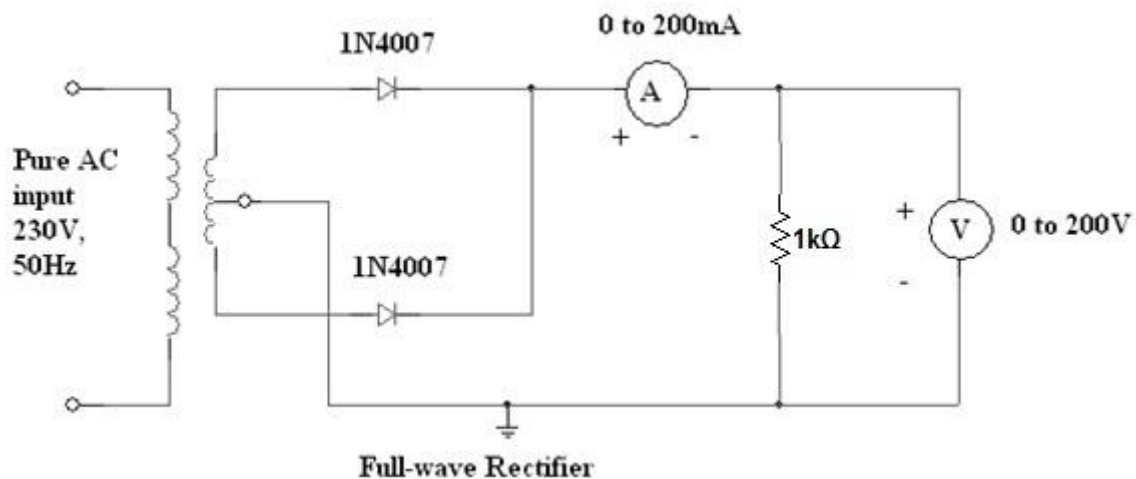
$$PIV_{HWR} = V_m$$

$$PIV_{FWR} = 2V_m$$

Comparison of Half-wave and Full-wave rectifier

S.No	Particulars	Type of Rectifier	
		Half-Wave	Full-Wave
1.	No. of diodes	1	2
2.	Maximum Rectification Efficiency	40.6%	81.2%
3.	$V_{d.c}$ (no load)	$\frac{V_m}{\pi}$	$\frac{2V_m}{\pi}$
4.	Ripple Factor	1.21	0.48
5.	Peak Inverse Voltage	V_m	$2V_m$
6.	Output Frequency	f	2f
7.	Transformer Utilization Factor	0.287	0.693

Circuit Diagram:**Half wave Rectifier (without filter):****Figure1: Circuit diagram of Half-wave rectifier**

Full Wave Rectifier (without filter):**Figure 2: Circuit diagram of Full wave rectifier****Procedure:****PART-I: Half wave rectifier without filter:**

1. Connect the circuit as shown in the figure-(1).
2. Connect the multimeter across the 1kΩ load.
3. Measure the AC and DC voltages by setting multimeter to ac and dc mode respectively.
4. Now calculate the ripple factor using the following formula.

$$\text{Ripple factor}(\gamma) = \frac{V_{AC}}{V_{DC}}$$

5. Connect the CRO channel-1 across input and channel-2 across output i.e load and Observe the input and output Waveforms.
6. Now calculate the peak voltage of input and output waveforms and also the frequency.

PART-II: Full wave rectifier without filter:

1. Connect the circuit as shown in the figure-(2).
2. Repeat the above steps 2-6
3. Plot different graphs for wave forms and ripple factor

Observations:

Table 1: Half wave rectifier without Filter

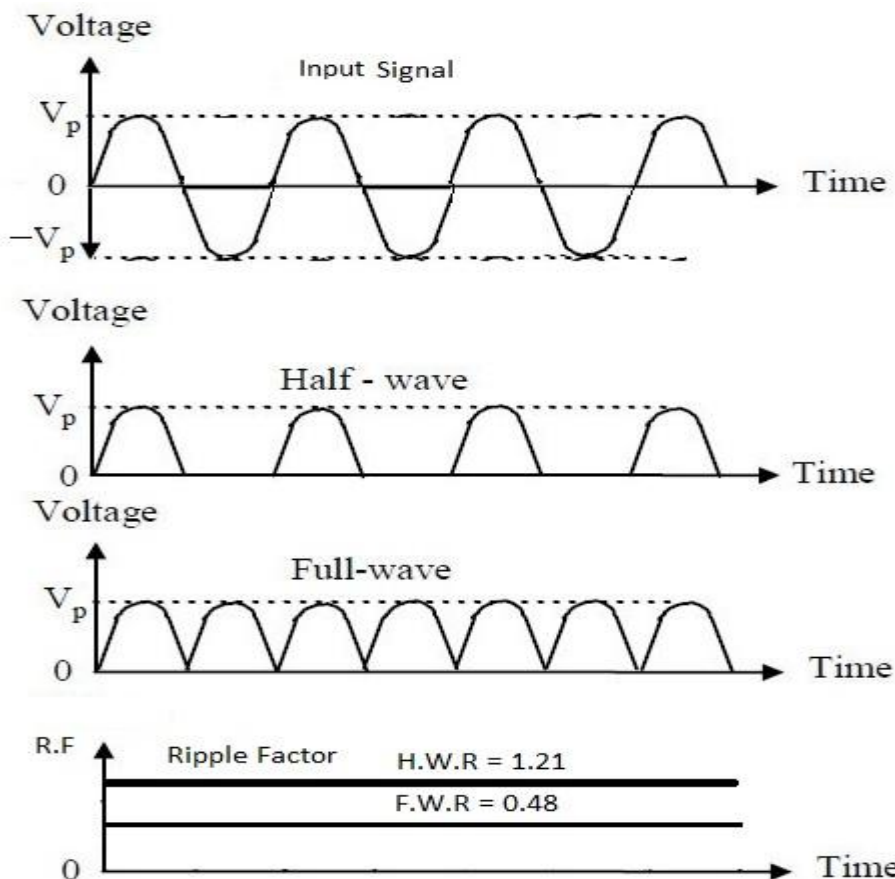
$V_{AC}(V)$	$V_{DC}(V)$	Ripple Factor $\gamma = \frac{V_{ac}}{V_{dc}}$	Input Signal			Output Signal	
			V_m p-p(v)	V_m peak(v)	Frequen cy (Hz)	V_m p-p(v)	Frequen cy (Hz)

Table 2: Full wave rectifier without Filter

$V_{AC}(V)$	$V_{DC}(V)$	Ripple Factor $\gamma = \frac{V_{ac}}{V_{dc}}$	Input Signal			Output Signal	
			V_m p-p(v)	V_{mpeak} (v)	Frequen cy (Hz)	V_m p-p(v)	Frequen cy (Hz)

Calculations:

1. Ripple Factor = $\gamma_{HWR} = \frac{V_{AC}}{V_{DC}}$
2. Percentage Regulation = $\frac{V_{NL} - V_{FL}}{V_{FL}} \times \%$

Expected Waveforms:**Result:**

1. Half Wave and Full Wave rectifier characteristics are studied.
2. Ripple factor of Half wave rectifier = -----
3. Ripple factor of Full wave rectifier = -----
4. Regulation of Half wave rectifier = -----
5. Regulation of Full wave rectifier = -----

Viva Questions:**1. What is a rectifier?**

Ans: A rectifier is an electrical device that converts alternating current (AC), which periodically reverses direction, to direct current (DC), which flows in only one direction. The process is known as rectification.

2. What is a ripple factor?

Ans: Ripple factor can be defined as the variation of the amplitude of DC (Direct current) due to improper filtering of AC power supply. it can be measured by $RF = V_{rms} / V_{dc}$

3. What is efficiency?

Ans: Rectifier efficiency is the ratio of the DC output power to the AC input power.

4. What is PIV?

Ans: The peak inverse voltage is either the specified maximum voltage that a [diode rectifier](#) can block, or, alternatively, the maximum that a rectifier needs to block in a given application.

5. What are the applications of rectifier?

Ans: The primary application of rectifiers is to derive DC power from an AC supply. Virtually all electronic devices require DC, so rectifiers are used inside the power supplies of virtually all electronic equipment. Rectifiers are also used for [detection](#) of [amplitude modulated](#) radio signals. Rectifiers are used to supply polarised voltage for [welding](#).

6. Give some rectifications technologies?

Ans: Synchronous rectifier, Vibrator, Motor-generator set, Electrolytic, Mercury arc, and Argon gas electron tube.

7. What is the efficiency of bridge rectifier?

Ans: 81 %

Experiment No:4**Half Wave and Full Wave Rectifier With Filter****Aim:** (i) To study the operation of a Half wave and Full wave rectifier with filters

(ii) To find its:

1. Ripple Factor
2. Percentage Regulation

Components:

Name	Quantity
Diodes 1N4007(Si)	2
Resistor $1K\Omega$	1
Capacitor $100\mu F$	2
Inductor (35 mH),	1

Equipment:

Name	Range	Quantity
CRO	0-1MHz	1
CRO probes	----	2
Multimeter	----	1
Transformer	220V/9V, 50Hz	1
Connecting Wires	----	----

Specifications:**Silicon Diode 1N4007:**

Max Forward Current = 1A

Max Reverse Current = $5.0\mu A$

Max Forward Voltage = 0.8V

Max Reverse Voltage = 1000V

Max Power Dissipation = 30mW

Temperature = -65 to 200° C

Theory:

A rectifier is a circuit that converts a pure AC signal into a pulsating DC signal or a signal that is a combination of AC and DC components.

In DC supplies, a rectifier is often followed by a filter circuit which converts the pulsating DC signal into pure DC signal by removing the AC component.

An L-section filter consists of an inductor and a capacitor connected in the form of an inverted L.

A π - section filter consists of two capacitors and one induction in the form symbol pi.

Ripple Factor:

Ripple factor is defined as the ratio of the effective value of AC components to the average DC value. It is denoted by the symbol ' γ '.

$$\gamma_{HWR \text{ L-section}} = \frac{V_{AC}}{V_{DC}} = \frac{\pi}{2\sqrt{2}} \frac{X_C}{X_L}$$

where $X_L = \omega L$, $X_C = \frac{1}{\omega C}$

$$\gamma_{FWR \pi\text{-section}} = \frac{V_{AC}}{V_{DC}} = \sqrt{2} \frac{X_{C1} X_{C2}}{R X_L}$$

where $X_L = 2\omega L$, $X_C = \frac{1}{2\omega C}$

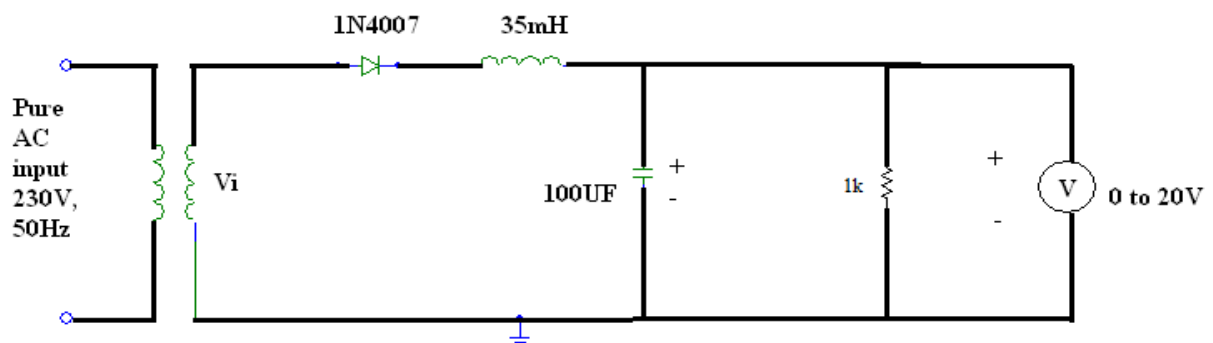
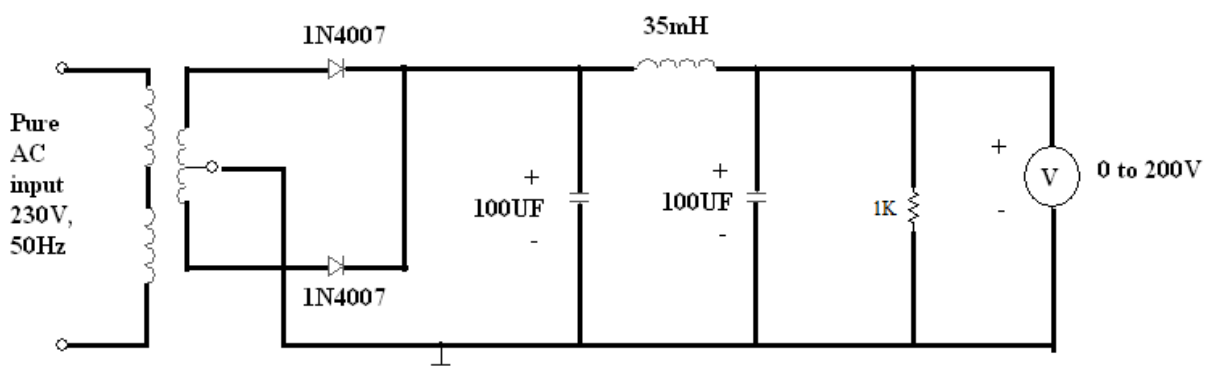
Circuit Diagram:**Half Wave Rectifier (with L-section filter):**

Figure 1: Half wave rectifier with L-section Filter

Full Wave Rectifier (with π -section filter):Figure 2: Full wave rectifier with π -section filter**Procedure:****PART-I:****Half wave rectifier with L-section filter:**

1. Connect the circuit as shown in the figure-(1).
2. Connect the multimeter across the $1k\Omega$ load.

- Measure the AC and DC voltages by setting multimeter to ac and dc mode respectively.
- Now calculate the ripple factor using the following formula.

$$\text{Ripple factor}(\gamma) = \frac{V_{AC}}{V_{DC}}$$

- Connect the CRO channel-1 across input and channel-2 across output i.e load and Observe the input and output Waveforms.
- Now calculate the peak voltage of input and output waveforms and also the frequency.

PART-II: Full wave rectifier with π -section filter:

- Connect the circuit with filter as shown in the figure-(2).
- Repeat the above steps 2-6

Observations:

Table 1: Half wave rectifier with L-section filter

$V_{AC}(V)$	$V_{DC}(V)$	Ripple Factor $\gamma = \frac{V_{ac}}{V_{dc}}$	Input Signal			Output Signal	
			V_m p-p(v)	V_m peak(v)	Frequen cy (Hz)	V_m p-p(v)	Frequen cy (Hz)

Table 2: Full wave rectifier with pi-Section filter

$V_{AC}(V)$	$V_{DC}(V)$	Ripple Factor $\gamma = \frac{V_{ac}}{V_{dc}}$	Input Signal			Output Signal	
			V_m p-p(v)	V_m peak(v)	Frequen cy (Hz)	V_m p-p(v)	Frequen cy (Hz)

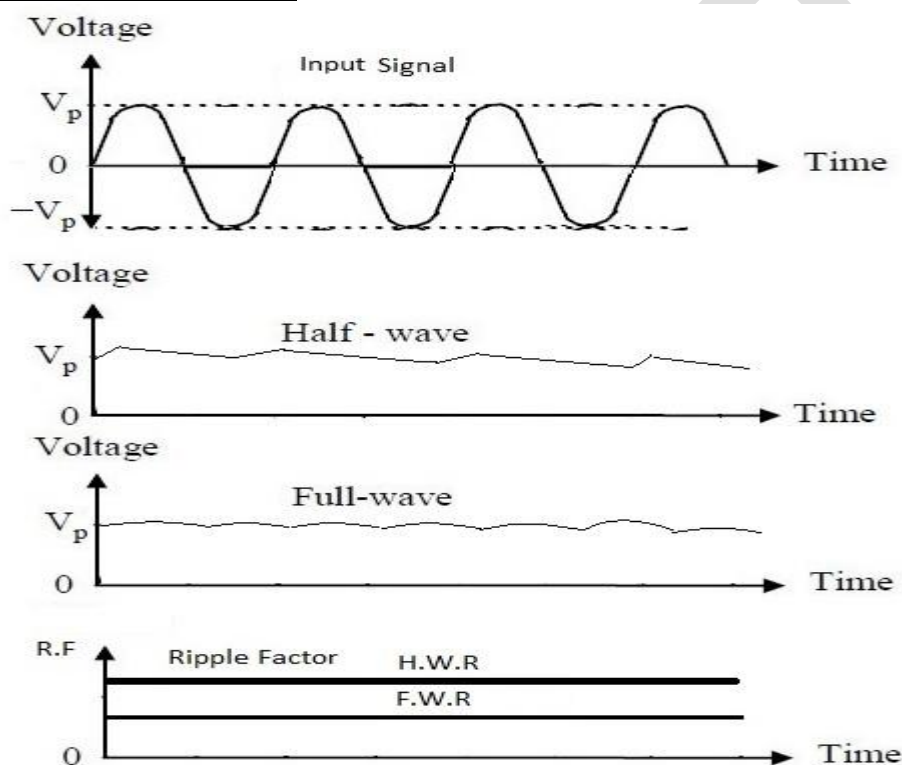
Calculations:

1. Ripple factor :

$$HWR_{L-SECTION} = \frac{V_{ac}}{V_{dc}}$$

$$FWR_{\pi-Section} = \frac{V_{ac}}{V_{dc}}$$

2. Percentage Regulation = $\frac{V_{DCNL} - V_{DCFL}}{V_{DCFL}} \times 100\%$

Expected Waveforms:**Result:**

1. Full Wave rectifier characteristics are studied.
2. Ripple factor of Half wave with L-section filter = -----
3. Ripple factor of Full wave with π -section filter = -----
4. Regulation of Half wave with L-section filter = -----
5. Regulation of Half wave with π -section filter = -----

Viva Questions:**1. What is filter ?**

Ans: Electronic [filters](#) are [electronic circuits](#) which perform [signal processing](#) functions, specifically to remove unwanted frequency components from the signal.

2. PIV center tapped FWR?

Ans: $2V_m$.

3. In filters capacitor is always connected in parallel, why?

Ans: Capacitor allows AC and blocks DC signal. In rectifier for converting AC to DC, capacitor is placed in parallel with output, where output is capacitor blocked voltage. If capacitance value increases its capacity also increases which increases efficiency of rectifier.

Experiment No:5

Characteristics of a BJT in Common Emitter Configuration

Aim:

4. To plot the Characteristics of a BJT in Common Emitter Configuration.
5. To measure the h-parameters of a BJT in Common Emitter Configuration.

Components:

Name	Quantity
Transistor BC 107	1
Resistor 1K Ω	2

Equipment:

Name	Range	Quantity
Bread Board		1
Regulated power supply	0-30V	2
Digital Ammeter	0-200mA/0-200 μ A	1
Digital Voltmeter	0-20V	2
Connecting Wires		

Specifications:**For Transistor BC 107:**

- Max Collector Current= 0.1A
- V_{CEO} max= 50V

Theory:

A BJT is called as Bipolar Junction Transistor and it is a three terminal active device which has emitter, base and collector as its terminals. It is called as a bipolar device because the flow of current through it is due to two types of carriers i.e., majority and minority carriers.

A transistor can be in any of the three configurations viz, Common base, Common emitter and Common Collector.

The relation between α , β , γ of CB, CE, CC are

$$\alpha = \frac{\beta}{1 + \beta} \quad \beta = \frac{\alpha}{1 - \alpha} \quad \gamma = 1 + \beta = \frac{1}{1 - \alpha}$$

In CE configuration base will be input node and collector will be the output node. Here emitter of the transistor is common to both input and output and hence the name common emitter configuration.

A transistor in CE configuration is used widely as an amplifier. While plotting the characteristics of a transistor the input voltage and output current are expressed as a function of input current and output voltage.

i.e., $V_{BE} = f(I_B, V_{CE})$ and

$$I_C = f(I_B, V_{CE})$$

Transistor characteristics are of two types.

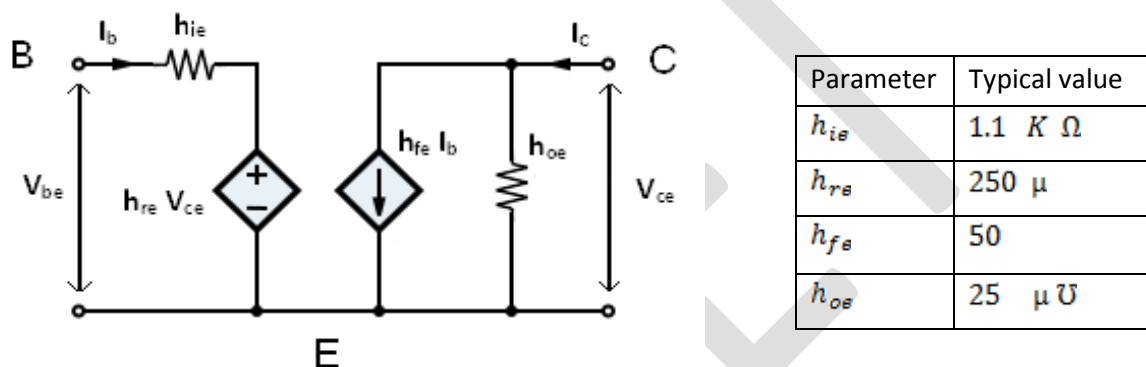
Input characteristics:- Input characteristics are obtained between the input current and input voltage at constant output voltage. It is plotted between V_{BE} and I_B at constant V_{CE} in CE configuration

Output characteristics:- Output characteristics are obtained between the output voltage and output current at constant input current. It is plotted between V_{CE} and I_C at constant I_B in CE configuration

The different regions of operation of the BJT are

J_E	J_C	REGION	APPLICATION
RB	RB	CUTT OFF	OFF SWITCH
FB	FB	SATURATION	ON SWITCH
FB	RB	ACTIVE	AMPLIFIER
RB	FB	REVERSE ACTIVE	ATTENUATOR

The Hybrid model of BJT and its typical values are as shown



The basic circuit diagram for studying input and output characteristics is shown in the circuit diagrams.

Circuit Diagram:

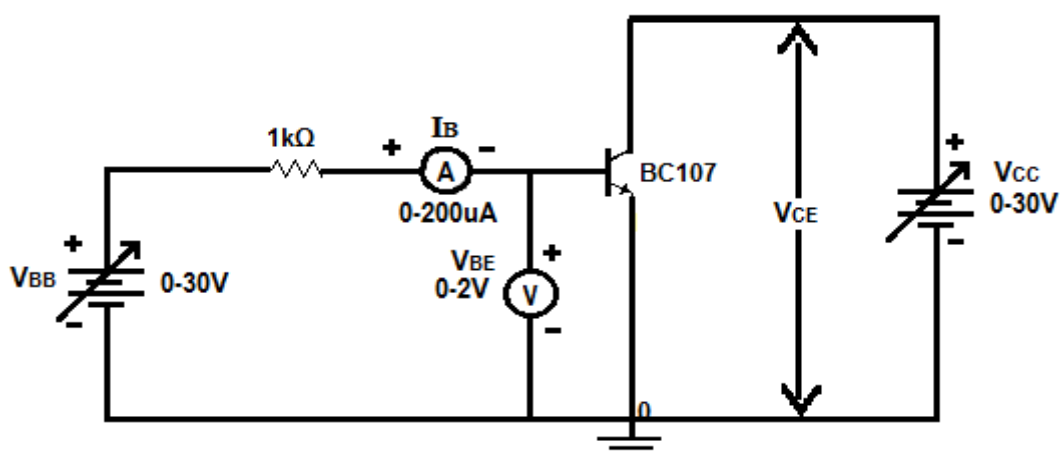


Fig.(1) - Input Characteristics:

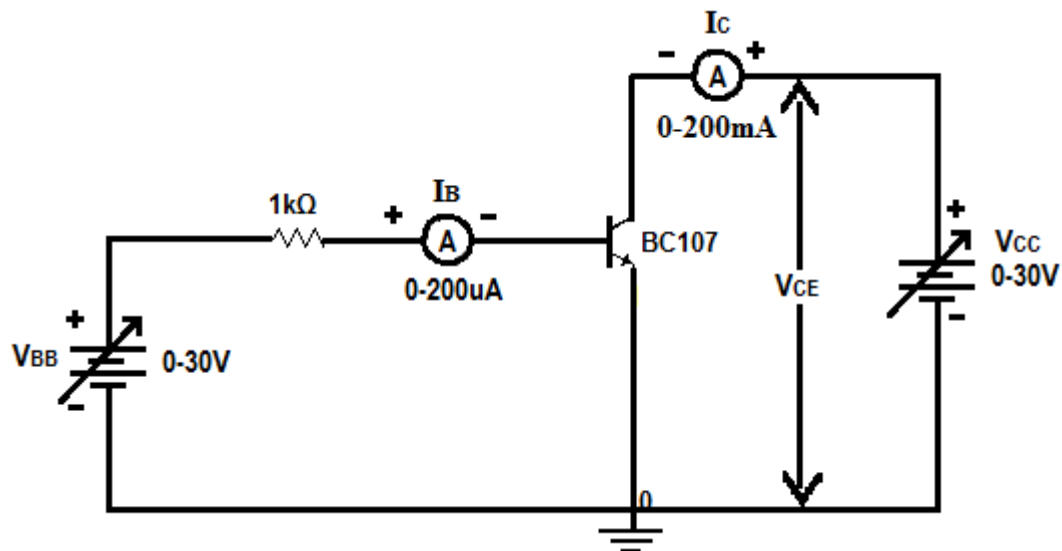
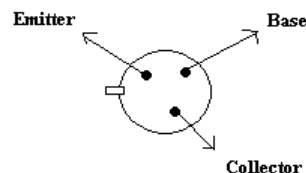


Fig. (2) - Output Characteristics

Pin assignment of Transistor:**Procedure:****Input Characteristics:**

- 1) Connect the circuit as shown in fig.(1). Adjust all the knobs of the power supply to their minimum positions before switching the supply on.
- 2) Adjust the V_{CE} to 0 V by adjusting the supply V_{CC} .
- 3) Vary the supply voltage V_{BB} so that V_{BE} varies in steps of 0.1 V from 0 to 0.5 V and then in steps of 0.02 V from 0.5 to 0.7 V. In each step note the value of base current I_B .
- 4) Adjust V_{CE} to 1, 2V and repeat step-3 for each value of V_{CE} .
- 5) Plot a graph between V_{BE} and I_B for different values of V_{CE} . These curves are called input characteristics

Output Characteristics:

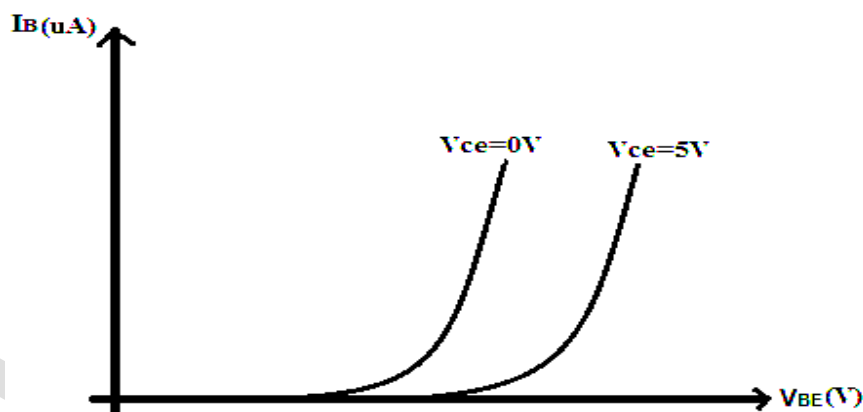
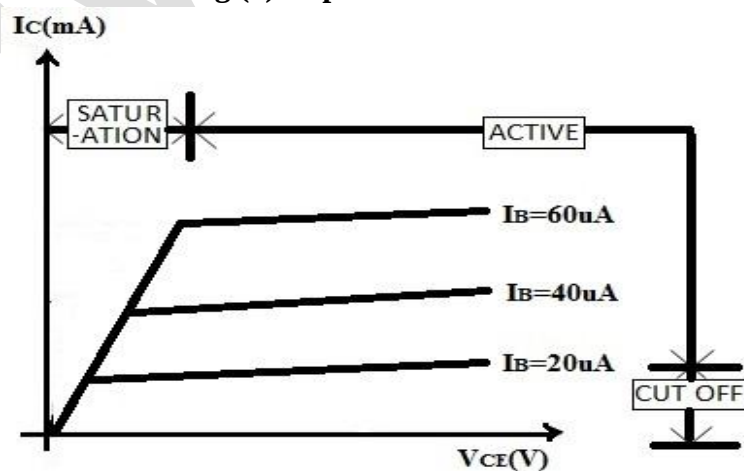
- 1) Connect the circuit as shown in fig. (2). All the knobs of the power supply must be at the minimum position before the supply is switched on.
- 2) Adjust the base current I_B to 20 μA by adjusting the supply V_{BB} .
- 3) Vary the supply voltage V_{CC} so that the voltage V_{CE} varies in steps of 0.2 V from 0 to 2 V and then in steps of 1 V from 2 to 10 V. In each step the base current should be adjusted to the present value and the collector current I_C should be recorded.
- 4) Adjust the base current at 40, 60 μA and repeat step-3 for each value of I_B .
- 5) Plot a graph between the output voltage V_{CE} and output current I_C for different values of the input current I_B . These curves are called the output characteristics.

Observations:**Table .(1) Input Characteristics**

$V_{CE} = 0V$		$V_{CE} = 5V$	
$V_{BE}(V)$	$I_B(\mu A)$	$V_{BE}(V)$	$I_B(\mu A)$

Table.(2) Output Characteristics

$I_B = 20\mu A$		$I_B = 40\mu A$		$I_B = 60\mu A$	
$V_{CE}(V)$	$I_C(mA)$	$V_{CE}(V)$	$I_C(mA)$	$V_{CE}(V)$	$I_C(mA)$

Graph:**Fig.(3). Input Characteristics****Fig.(4). Output Characteristics**

Calculations from Graph:

1. **Input Impedance (h_{ie}):** It is ratio of input base voltage (V_{BE}) to the change in input base current(I_B) with the output collector voltage (V_{CE}) kept constant. It is the slope of the input characteristics I_B vs V_{BE} .

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} , V_{CE} \text{ Constant } (\Omega)$$

Therefore,

2. **Reverse voltage gain (h_{re}):** It is the ratio of the change in the input base voltage (V_{BE}) and the corresponding change in output collector(I_C) voltage with constant input base current(I_B). It is the slope of V_{BE} vs V_{CE} curve.

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}} , I_B \text{ constant}$$

Therefore,

3. **Forward Current Gain (h_{fe}):** It is the ratio of the change in the output collector current(I_C) to the corresponding change in the input base current (I_B) keeping output collector voltage (V_{CE}) constant. It is the slope of I_C vs I_B curve .

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B} , V_{CE} \text{ Constant}$$

Therefore,

4. **Output Admittance (h_{oe}):** It is the ratio of change in the output collector current (I_C) to the corresponding change in the output collector voltage(V_{CE}) with the input base current (I_B) kept constant. It is the slope of the output characteristics V_{CE} vs I_C

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}} , I_B \text{ constant } (\Omega)$$

Therefore,

Inference:

1. Medium input and output resistances.
2. Smaller values if V_{CE} comes earlier cut-in-voltage.
3. Increase in the value of I_B causes saturation of the transistor of an earlier voltage.

Precautions:

1. While performing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.
2. Connect voltmeter and ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base and collector terminals of the transistor.

Result:

1. Input and output Characteristics of a BJT in Common Emitter Configuration are studied.
2. Measured the h-parameters of a BJT in Common Emitter Configuration.

Viva Questions:**1. Can we replace transistor by two back to back connected diodes?**

Ans: No, because the doping levels of emitter(heavily doped), base(lightly doped) and collector(doping level greater than base and less than emitter) terminals are different from p and n terminals in diode.

2. For amplification CE is preferred, why?

Ans: Because amplification factor beta is usually ranges from 20-500 hence this configuration gives appreciable current gain as well as voltage gain at its output on the other hand in the Common Collector configuration has very high input resistance($\sim 750K\Omega$) & very low output resistance($\sim 25\Omega$) so the voltage gain is always less than one & its most important application is for impedance matching for driving from low impedance load to high impedance source

3. To operate a transistor as amplifier, emitter junction is forward biased and collector junction is reverse biased, why?

Ans: Voltage is directly proportional to Resistance. Forward bias resistance is very less compared to reverse bias. In amplifier input forward biased and output reverse biased so voltage at output increases with reverse bias resistance.

4. Which transistor configuration provides a phase reversal between the input and output signals?

Ans: Common emitter configuration (180 DEG)

5. What is the range of β ?

Ans: Beta is usually ranges from 20-500

Experiment No:6

JFET Characteristics

Aim: 1.To study Drain Characteristics and Transfer Characteristics of a Junction Field Effect Transistor (JFET).

2.To measure drain resistance, transconductance and amplification factor.

Components:

Name	Quantity
JFET BFW 11	1
Resistor $100\text{K}\Omega, 1\text{K}\Omega$	2

Equipment:

Name	Range	Quantity
Bread Board		1
Regulated power supply	0-30V	1
Digital Ammeter	0-200mA	1
Digital Voltmeter	0-20V	2
Connecting Wires		

Specifications:

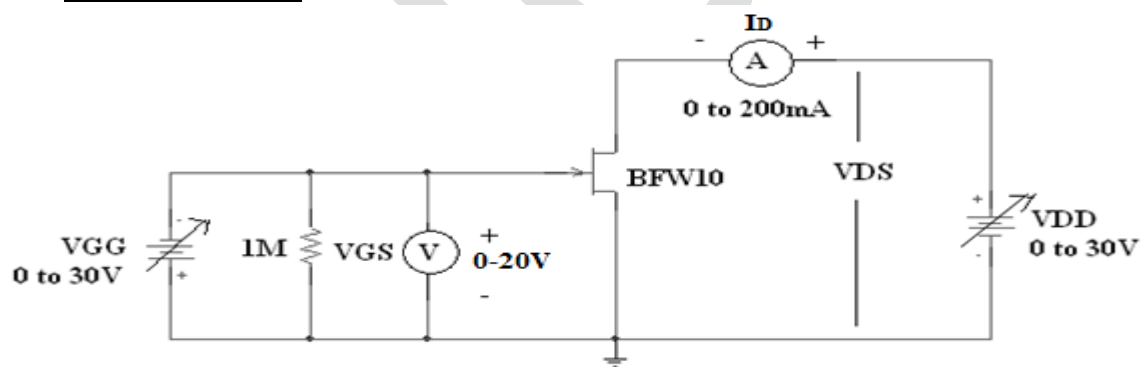
For FET BFW11:

Gate Source Voltage $V_{GS} = -30\text{V}$

Forward Gain Current $I_{GF} = 10\text{mA}$

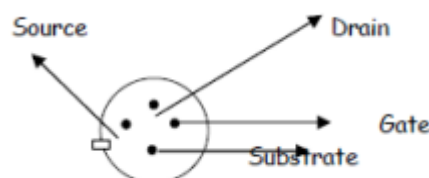
Maximum Power Dissipation $P_D = 300\text{mW}$

Circuit Diagram:



Fig(1).Characteristics of FET

Pin assignment of FET:



Theory:

The basic circuit diagram for studying drain and transfer characteristics is shown in the circuit diagram.

1. Drain characteristics are obtained between the drain to source voltage (V_{DS}) and drain current (I_D) taking gate to source voltage (V_{GS}) as the parameter.

- Transfer characteristics are obtained between the gate to source voltage (V_{GS}) and drain current (I_D) taking drain to source voltage (V_{DS}) as the parameter.

Procedure:**Drain Characteristics:**

- Connect the circuit as shown in the circuit diagram.
- Keep $V_{GS} = 0V$ by varying V_{GG} .
- Varying V_{DD} gradually, note down drain current I_D and drain to source voltage (V_{DS}).
- Step size is not fixed because of non linear curve and vary the X-axis variable (i.e. if output variation is more, decrease input step size and vice versa).
- Repeat above procedure (step 3) for $V_{GS} = -1V$.

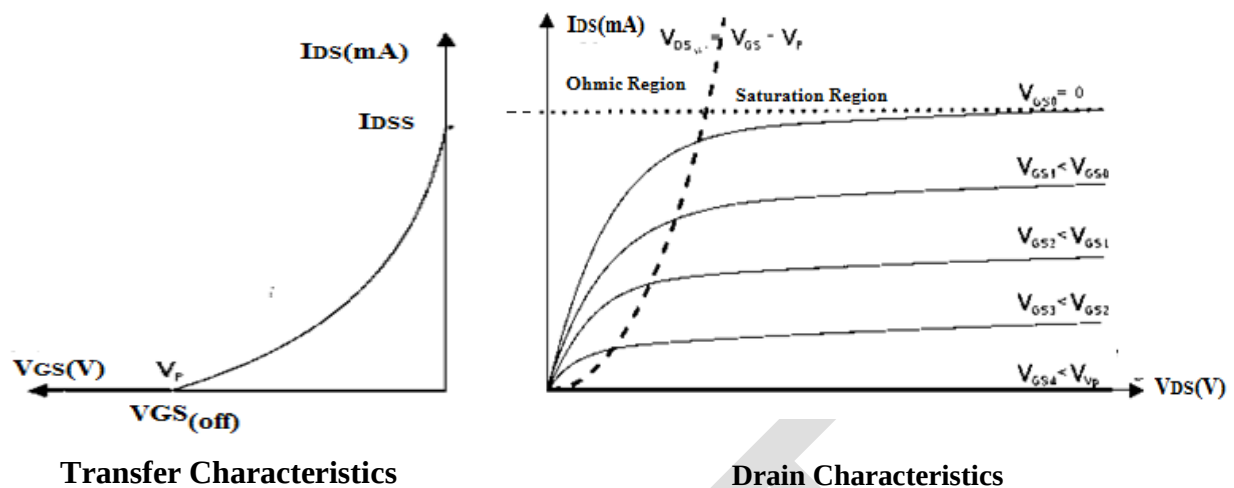
Transfer Characteristics:

- Connect the circuit as shown in the circuit diagram.
- Keep $V_{DS} = 2V$ by varying V_{DD} .
- Varying V_{GG} gradually, note down both drain current I_D and gate-source voltage (V_{GS}).
- Step size is not fixed because of non linear curve and vary the X-axis variable (i.e. if output variation is more, decrease input step size and vice versa).
- Repeat above procedure (step 3) for $V_{DS} = 4V$.

Observations:

Drain Characteristics			
$V_{GS} = 0V$		$V_{GS} = -1V$	
$V_{DS}(V)$	$I_D(mA)$	$V_{DS}(V)$	$I_D(mA)$

Transfer Characteristics			
$V_{DS} = 2V$		$V_{DS} = 4V$	
$V_{GS}(V)$	$I_D(mA)$	$V_{GS}(V)$	$I_D(mA)$

Graph:

1. Plot the drain characteristics by taking V_{DS} on X-axis and I_D on Y-axis at a constant V_{GS} .
2. Plot the transfer characteristics by taking V_{GS} on X-axis and taking I_D on Y-axis at constant V_{DS} .

Calculations from Graph:

1. **Drain Resistance (r_d):** It is given by the relation of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in Drain Current (ΔI_D) for a constant gate to source voltage (ΔV_{GS}), when the JFET is operating in pinch-off region.
2. **Trans Conductance (g_m):** Ratio of small change in drain current (ΔI_D) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant V_{DS} .

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS} \text{ (from transfer characteristics).}$$

The value of **gm** is expressed in mho's ($\bar{U}$) or Siemens (s).

3. **Amplification factor (μ):** It is given by the ratio of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant drain current (I_D).

$$\mu = \left(\frac{\Delta V_{DS}}{\Delta I_D} \right) * \left(\frac{\Delta I_D}{\Delta V_{GS}} \right) = \frac{\Delta V_{DS}}{\Delta V_{GS}} = r_d * g_m$$

Inference:

1. As the gate to source voltage (V_{GS}) is increased above zero, pinch off voltage is increased at a smaller value of drain current as compared to that when $V_{GS} = 0V$.
2. The value of drain to source voltage (V_{DS}) is decreased as compared to that when $V_{GS} = 0V$.

Precautions:

1. While performing the experiment do not exceed the ratings of the FET. This may lead to damage the FET.
2. Connect voltmeter and ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the Source, Drain and Gate terminals of the transistor.

Result:

1. Drain Characteristics and Transfer Characteristics of a Field Effect Transistor are studied (FET).
2. Measured drain resistance, transconductance and amplification factor.

Viva Questions:**1. Why FET is called a Unipolar device?**

Ans: FETs are unipolar transistors as they involve single-carrier-type operation.

2. What are the advantages of FET?

Ans: The main advantage of the FET is its high input resistance, on the order of 100 MΩ or more. Thus, it is a voltage-controlled device, and shows a high degree of isolation between input and output. It is a unipolar device, depending only upon majority current flow. It is less noisy, and is thus found in FM tuners and in low-noise amplifiers for VHF and satellite receivers. It is relatively immune to radiation. It exhibits no offset voltage at zero drain current and hence makes an excellent signal chopper. It typically has better thermal stability than a bipolar junction transistor (BJT)

3. What is transconductance?

Ans: Transconductance is an expression of the performance of a bipolar transistor or field-effect transistor (FET). In general, the larger the transconductance figure for a device, the greater the gain (amplification) it is capable of delivering, when all other factors are held constant. The symbol for transconductance is g_m . The unit is the siemens, the same unit that is used for direct-current (DC) conductance.

4. What are the disadvantages of FET?

Ans: It has a relatively low gain-bandwidth product compared to a BJT. The MOSFET has a drawback of being very susceptible to overload voltages, thus requiring special handling during installation. The fragile insulating layer of the MOSFET between the gate and channel makes it vulnerable to electrostatic damage during handling. This is not usually a problem after the device has been installed in a properly designed circuit.

5. Relation between μ , g_m and r_d ?

Ans: $\mu = g_m * r_d$

EXPERIMENT NO: 7

STUDY OF CRO, MEASUREMENT OF AMPLITUDE & FREQUENCY

Aim: Study of CRO and to find the Amplitude and Frequency using CRO.

Components and Equipments Required: Cathode-ray oscilloscope, Function Generator, CRO Probes and Bread Board

Theory:

An outline explanation of how an oscilloscope works can be given using the block diagram shown below:

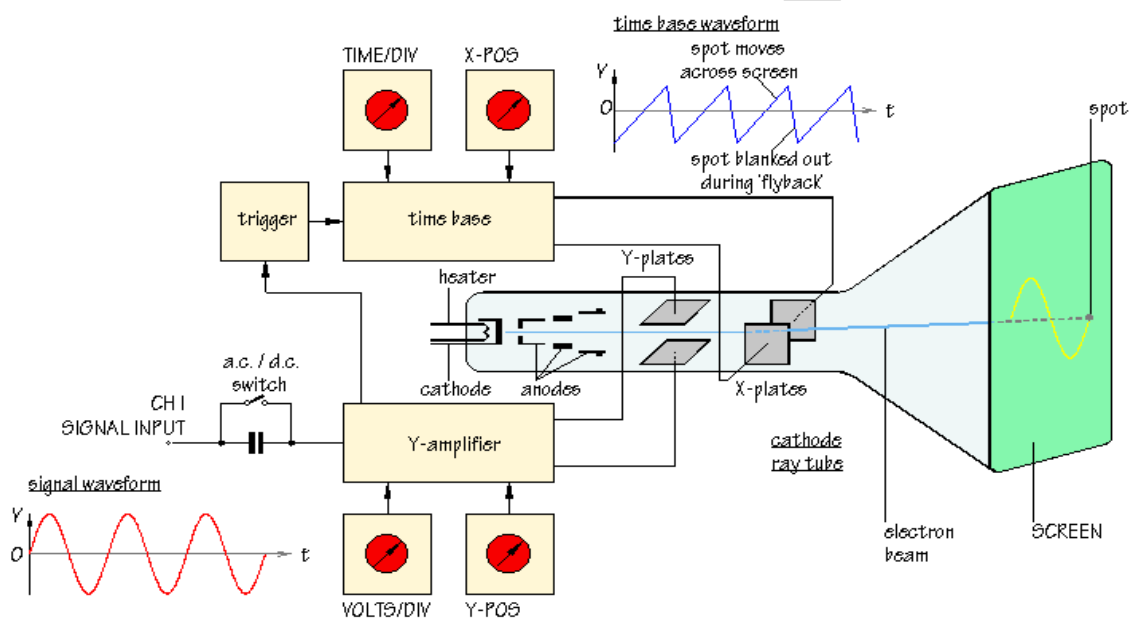


Fig 1: Cathode Ray Oscilloscope

Like a television screen, the screen of an oscilloscope consists of a **cathode ray tube**. Although the size and shape are different, the operating principle is the same. Inside the tube is a vacuum. The electron beam emitted by the heated cathode at the rear end of the tube is accelerated and focused by one or more anodes, and strikes the front of the tube, producing a bright spot on the phosphorescent screen.

The electron beam is bent, or deflected, by voltages applied to two sets of plates fixed in the tube. The horizontal deflection plates or **X-plates** produce side to side movement. As you can see, they are linked to a system block called the **time base**. This produces a saw tooth waveform. During the rising phase of the saw tooth, the spot is driven at a uniform rate from left to right across the front of the screen. During the falling phase, the electron beam returns rapidly from right to left, but the spot is 'blanked out' so that nothing appears on the screen. In this way, the time base generates the X-axis of the V/t graph.

The slope of the rising phase varies with the frequency of the saw tooth and can be adjusted, using the TIME/DIV control, to change the scale of the X-axis. Dividing the oscilloscope screen into squares allows the horizontal scale to be expressed in seconds, milliseconds or microseconds per division (s/DIV, ms/DIV, μ s/DIV). Alternatively, if the squares are 1 cm apart, the scale may be given as s/cm, ms/cm or μ s/cm.

The signal to be displayed is connected to the **input**. The AC/DC switch is usually kept in the DC position (switch closed) so that there is a direct connection to the **Y-amplifier**. In the AC position (switch open) a capacitor is placed in the signal path. The capacitor blocks DC signals but allows AC signals to pass.

The Y-amplifier is linked in turn to a pair of **Y-plates** so that it provides the Y-axis of the V/t graph. The overall gain of the Y-amplifier can be adjusted, using the VOLTS/DIV control, so that the resulting display is neither too small or too large, but fits the screen and can be seen clearly. The vertical scale is usually given in V/DIV or mV/DIV.

The **trigger** circuit is used to delay the time base waveform so that the same section of the input signal is displayed on the screen each time the spot moves across. The effect of this is to give a stable picture on the oscilloscope screen, making it easier to measure and interpret the signal.

Changing the scales of the X-axis and Y-axis allows many different signals to be displayed. Sometimes, it is also useful to be able to change the *positions* of the axes. This is possible using the **X-POS** and **Y-POS** controls. For example, with no signal applied, the normal trace is a straight line across the centre of the screen. Adjusting Y-POS allows the zero level on the Y-axis to be changed, moving the whole trace up or down on the screen to give an effective display of signals like pulse waveforms which do not alternate between positive and negative values.

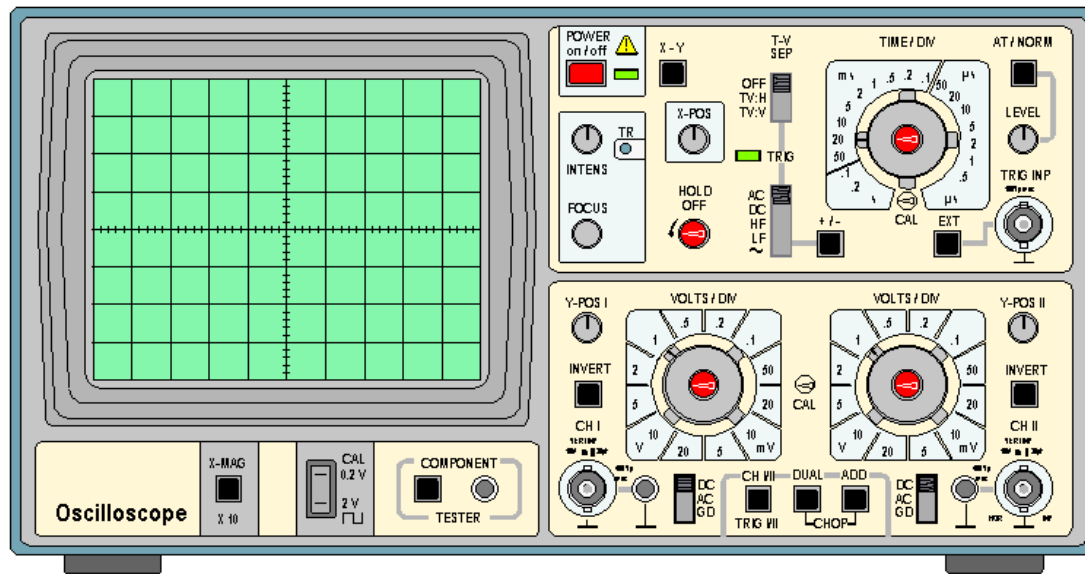


Fig 2: Front View of Oscilloscope

Screen: Usually displays a V/t graph, with voltage V on the vertical axis and time t on the horizontal axis. The scales of both axes can be changed to display a huge variety of signals.

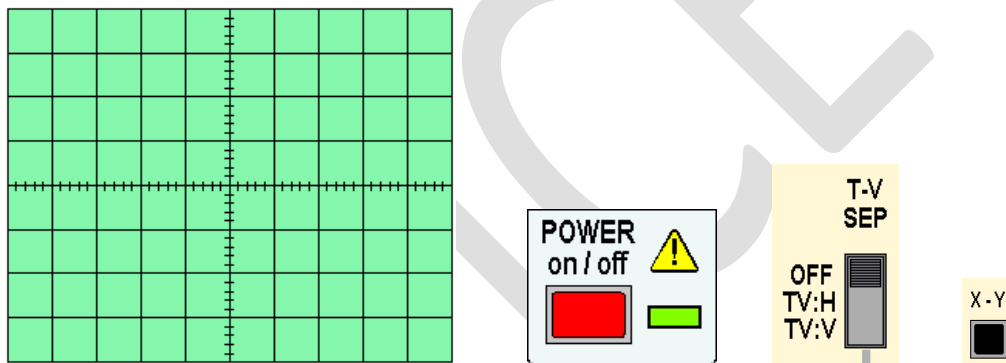


Fig 3: Screen display of Oscilloscope

On/Off Switch: Pushed in to switch the oscilloscope on. The green LED illuminates.

X-Y Control: Normally in the OUT position.

When the X-Y button is pressed IN, the oscilloscope does not display a V/t graph. Instead, the vertical axis is controlled by the input signal to CH II. This allows the oscilloscope to be used to display a V/V voltage/voltage graph.

The X-Y control is used when you want to display component characteristic curves, or Lissajous figures. (Links to these topics will be added later.)

TV-Separation: Oscilloscopes are often used to investigate waveforms inside television systems. This control allows the display to be synchronised with the television system so that the signals from different points can be compared.

Time / Div: Allows the horizontal scale of the V/t graph to be changed.

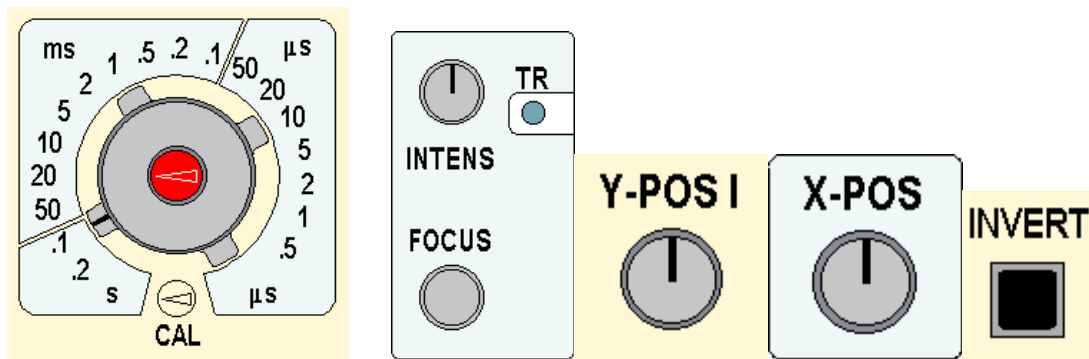


Fig 4: Time division, Intensity, focus, X-Y mode knobs

With more experience of using the oscilloscope, you will develop a clear understanding of the functions of the important trigger controls and be able to use them effectively.

Intensity And Focus: Adjusting the INTENSITY control changes the brightness of the oscilloscope display. The FOCUS should be set to produce a bright clear trace.

If required, TR can be adjusted using a small screwdriver so that the oscilloscope trace is exactly horizontal when no signal is connected.

X-POS: Allows the whole V/t graph to be moved from side to side on the oscilloscope screen.

This is useful when you want to use the grid in front of the screen to make measurements, for example, to measure the period of a waveform.

Y-POS I And Y-POS II: These controls allow the corresponding trace to be moved up or down, changing the position representing 0 V on the oscilloscope screen.

To investigate an alternating signal, you adjust Y-POS so that the 0 V level is close to the centre of the screen. For a pulse waveform, it is more useful to have 0 V close to the bottom of the screen. Y-POS I and Y-POS II allow the 0 V levels of the two traces to be adjusted independently.

Invert: When the INVERT button is pressed IN, the corresponding signal is turned upside down, or inverted, on the oscilloscope screen. This feature is sometimes useful when comparing signals.

CH I And CH II Inputs: Signals are connected to the BNC input sockets using BNC plugs.

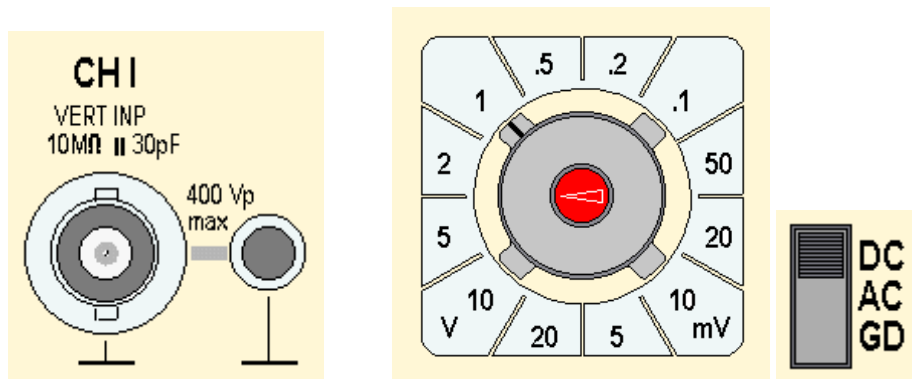


Fig 5: Voltage division, Channels, AC, DC and GD knobs

The smaller socket next to the BNC input socket provides an additional 0 V, GROUND or EARTH connection.

Volts / Div: Adjust the vertical scale of the V/t graph. The vertical scales for CH I and CH II can be adjusted independently.

DC/AC/GND Slide Switches: In the DC position, the signal input is connected directly to the Y-amplifier of the corresponding channel, CH I or CH II. In the AC position, a capacitor is connected into the signal pathway so that DC voltages are blocked and only changing AC signals are displayed.

In the GND position, the input of the Y-amplifier is connected to 0 V. This allows you to check the position of 0 V on the oscilloscope screen. The DC position of these switches is correct for most signals.

Trace Selection Switches: The settings of these switches control which traces appear on the oscilloscope screen.

Measurement of Amplitude & Frequency:

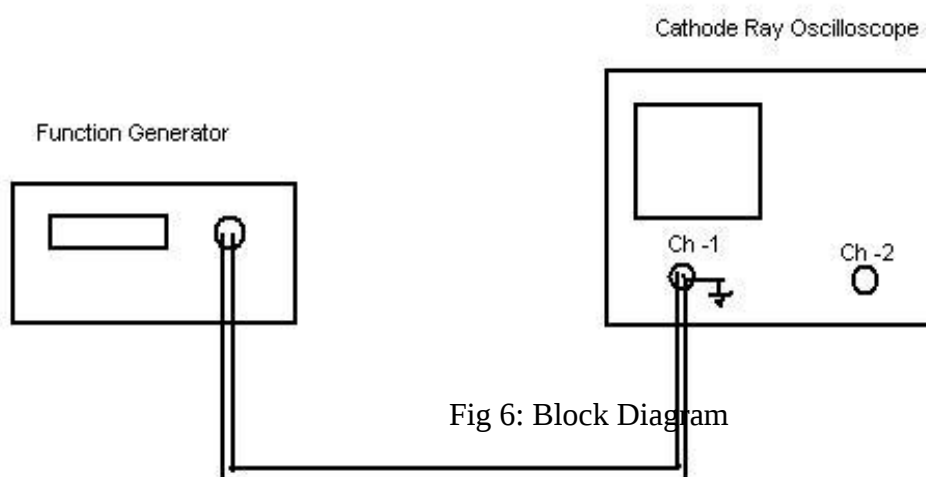


Fig 6: Block Diagram

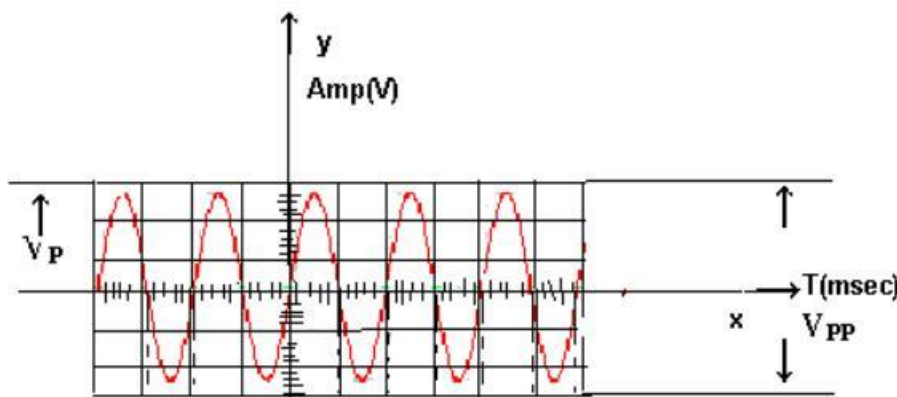
Model waveforms:

Fig 7: Sinusoidal waveform

A) Measurement of Amplitude:**Procedure:**

1. Make the connections as per the diagram shown above.
2. Put the CRO on a single channel mode and bring the CRO into operation by adjusting the trace of the beam to a normal brightness and into a thin line.
3. Now apply the sinusoidal wave of different amplitudes by using the LEVEL and COARSE buttons of the function generator.
4. Note on the vertical scale the peak to peak amplitude (V_{pp}).

Observations:

S.NO	No.of Vertical Divisions(X)	Voltage/ Division (Y)	$V_{p-p}=X*Y$	$V_m=V_{p-p}/2$

B) Measurement of Frequency:**Procedure:**

- Make the connections as per the diagram shown above.
- Put the CRO on a single channel mode and bring the CRO into operation by adjusting the trace of the beam to a normal brightness and into a thin line.
- Now apply the sinusoidal wave of different frequencies by using the LEVEL and COARSE buttons of the function generator.

- Note on the an horizontal scale period (T) in second by observing difference between the two successive peaks of the waveform.

Observations:

S.NO	No.Of Horizontal Divisions(X)	Time/Division (Y)	$T=X*Y$	$f=1/T$

C) Component Testing:**Procedure**

- Switch on the CRO, Insert component terminals in Component Tester (CT) sockets
- Press x-y mode and CT switches
- Note down the Pattern from display.

Observations:

S.NO	Component	Signature or Pattern

Results:

- Measured voltage amplitude and frequency of given signal successfully
- Tested given components using Component tester of CRO.

Experiment No:8 BJT Biasing

Aim:- To design a fixed bias, collector to base bias and a self bias circuit and determine their stability factors experimentally.

Components:

Name	Quantity
Transistor (BEL100N),	1
Resistors (from design)	1

Equipment:

Name	Range	Quantity
Bread board		1
Regulated power supply	0-30V	1
Soldering iron		1
Digital Ammeter	0-200 μ A/200mA	1
Digital Voltmeter	0-20V	1
Connecting Wires		

Specifications:

BJT Transistor BEL100N:

Max Collector base voltage (open emitter) $V_{CBO} = 60V$

Max Emitter base voltage (open collector) $V_{EBO} = 7V$

Max Collector current (d.c.) = 500mA

Max Junction Temperature = 200°C

Max Total Power Dissipation = 0.8W

D.C. Current gain at $I_C = 150mA$, $V_{CE} = 1V$ $h_{fe} = 50$ to 280

Theory:

A transistor acts as an amplifier in active region. Biasing circuit is used in a transistor to keep in the active region. Following are the three common biasing circuits used in transistors.

- 1) Fixed bias circuit:- It is named so because it provides a fixed value of base current for given values of V_{CC} and R_b .
- 2) Collector to base bias circuit:- In this circuit a the base bias is taken from the collector by connecting a resistor between base and collector.
- 3) Self bias circuit:- In this circuit the base bias is obtained by using a voltage divider network. An emitter resistor is used to keep the collector current and hence the Q-point stable.

Stability factor is defined as the rate of change of collector current with reverse saturation current. For a stable Q-point it should be as small as possible. A self bias circuit provides the least stability factor and hence it is commonly preferred over other biasing circuits.

Stability factor is mathematically given by the following equation.

$$S = \frac{1 + \beta}{1 - \beta \times \frac{\partial I_B}{\partial I_C}}$$

(a) Fixed bias

$$s = 1 + \beta$$

(b) Collector to base bias

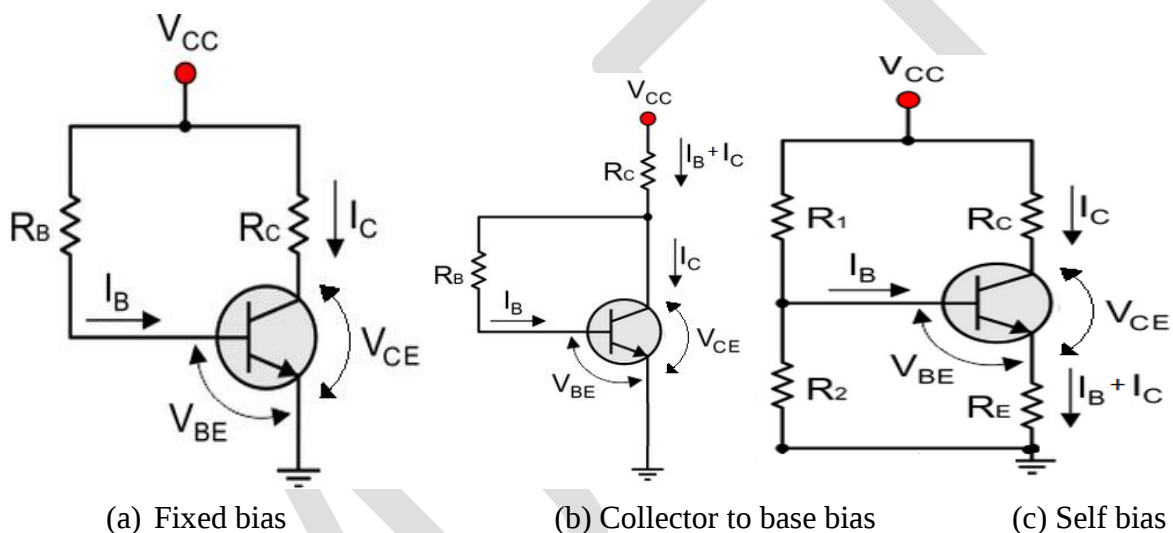
$$S = \frac{1 + \beta}{1 + \beta \frac{R_c}{R_b + R_c}}$$

(c) Self bias

$$S = \frac{1 + \beta}{1 + \beta \frac{R_E}{R_b + R_E}}$$

Design:Given $V_{CC} = 12V$ $V_{CE} = 6V$ $I_C = 1mA$ $\beta = 100$

- Design a fixed bias circuit.
- Design a collector to base bias circuit.
- Design a self bias circuit.

Circuit diagram:

- Design a fixed bias circuit to establish the Q-point at $I_C = 1.5mA$, $V_{CE} = 6V$. Use a transistor with $\beta = 100$ and $V_{BE} = 0.65V$. Given $V_{CC} = 12V$.

Solution: $I_B = \frac{I_C}{\beta} = \frac{1.5 \times 10^{-3}}{100} = 15\mu A$

Apply KVL to the loop consisting of V_{CC} , R_b and V_{BE} .

$$-V_{CC} + I_B \times R_b + V_{BE} = 0$$

$$\Rightarrow R_b = 760 \text{ K}\Omega$$

Apply KVL to the loop consisting of V_{CC} , R_C , and V_{CE} .

$$-V_{CC} + I_C \times R_C + V_{CE} = 0$$

$$\Rightarrow R_C = 4 \text{ K}\Omega$$

- b) Design a Collector to base bias circuit to establish the Q-point at $I_C = 1.5\text{mA}$, $V_{CE} = 6\text{V}$. Use a transistor with $\beta = 100$ and $V_{BE} = 0.65\text{V}$. Given $V_{CC} = 12\text{V}$.

Solution: $I_B = \frac{I_C}{\beta} = \frac{1.5 \times 10^{-3}}{100} = 15\mu\text{A}$

Apply KVL to the loop consisting of V_{CC} , R_C , and V_{CE} .

$$-V_{CC} + (I_C + I_B) \times R_C + V_{CE} = 0$$

$$\Rightarrow R_C = 3.96 \text{ K}\Omega$$

Apply KVL to the loop consisting of V_{CC} , R_b and V_{BE} .

$$-V_{CC} + (I_C + I_B) \times R_C + I_B \times R_b + V_{BE} = 0$$

$$\Rightarrow R_b = 357 \text{ K}\Omega$$

- c) Design a self bias circuit to establish the Q-point at $I_C = 1.5\text{mA}$ and $V_{CE} = 4\text{V}$. Use a transistor with $\beta = 100$ and $V_{BE} = 0.65\text{V}$. Given $V_{CC} = 12\text{V}$, $R_C = 3.9\text{K}\Omega$.

Solution: $I_B = \frac{I_C}{\beta} = \frac{1.5 \times 10^{-3}}{100} = 15\mu\text{A}$

Apply KVL to the loop consisting of V_{CC} , R_C , V_{CE} and R_E .

$$-V_{CC} + I_C \times R_C + V_{CE} - I_E \times R_E = 0$$

$$\Rightarrow R_E = 1.42 \text{ K}\Omega$$

Apply Thevenin's theorem to the base circuit.

$$V_{th} = V_b = \frac{V_{CC} \times R_2}{R_1 + R_2} \text{ and } R_{th} = R_b = \frac{R_1 \times R_2}{R_1 + R_2}$$

We know that the stability factor for a self bias circuit is given by,

$$S = \frac{1 + \beta}{1 + \beta \frac{R_E}{R_b + R_E}}$$

$$\Rightarrow R_b = 15.94 \text{ K}\Omega$$

apply KVL to the base circuit loop:

$$-V_b + I_B \times R_b + V_{BE} + I_E \times R_E = 0$$

$$V_b = 3.04\text{V}$$

Now divide R_b with V_b ,

$$R_1 = \frac{V_{CC} \times R_b}{V_b} = 63 \text{ K}\Omega$$

$$\text{Also, } R_b = \frac{R_1 \times R_2}{R_1 + R_2} \Rightarrow R_2 = 21.3 \text{ K}\Omega$$

Procedure:

- 1) Connect the fixed bias circuit as shown in figure (a).
- 2) Note the DC conditions ie, the values of V_{CE} , V_{BE} , I_C and I_B .
- 3) Heat the transistor by placing a soldering iron in its vicinity for a minute. Note the values of I_C and I_B .
- 4) Calculate the stability factor as mentioned in theory.
- 5) Repeat the above steps for collector to base bias and self bias circuits.

- 6) Calculate the stability factors theoretically and compare them with the practical values.

Observations:

Circuit	I_B (μA)		I_C (mA)		$\frac{\Delta I_B}{\Delta I_C}$	$S = \frac{1 + \beta}{1 - \beta \times \frac{\Delta I_B}{\Delta I_C}}$	S (Theoretical)
	I_{B1}	I_{B2}	I_{C1}	I_{C2}			
Fixed bias circuit							
Collector to Base bias circuit							
Self bias circuit							

Result:

Stability factors are calculated for each circuit. Theoretical and practical values of the stability factors are verified.

Experiment No: 9 Common Emitter Amplifier

Aim:

1. To plot the frequency response of a Common Emitter BJT amplifier.
2. To find the input and output impedances of the CE amplifier.
3. To find the cut off frequencies, Bandwidth and calculate its gain.

Components:

Name	Quantity
Transistor BC107	1
Resistor $100\text{K}\Omega$, $10\text{K}\Omega$, $2.2\text{K}\Omega$, $1\text{K}\Omega$	1, 1, 2, 1
Capacitor $10\mu\text{F}$, $100\mu\text{F}$	2, 1

Equipment:

Name	Range	Quantity
Bread Board		1
Dual power supply	0-30V	1
CRO	(0-20)MHz	1
Function Generator	(0-1)MHz	1
Connecting Wires		

Specifications:**For Transistor BC 107:**

- Max Collector Current= 0.1A
- $V_{ce0 \text{ max}} = 50\text{V}$

Theory:

The common emitter configuration is widely used as a basic amplifier as it has both voltage and current amplification.

Resistors R1 and R2 form a voltage divider across the base of the transistor. The function of this network is to provide necessary bias condition and ensure that emitter-base junction is operating in the proper region.

In order to operate transistor as an amplifier, the biasing is done in such a way that the operating point should be in the active region. For an amplifier the Q-point is placed so that the load line is bisected. Therefore, in practical design is always set to $V_{cc}/2$. This will confirm that the Q-point always swings within the active region. This limitation can be explained by maximum signal handling capacity. Output is produced without any clipping or distortion for the maximum input signal. If not so reduce the input signal magnitude.

The Bypass Capacitor:

The emitter resistor is required to obtain the DC quiescent stability. However the inclusion of it in the circuit causes a decrease in amplification at higher frequencies. In order to avoid such a condition, it is bypassed by capacitor so that it acts as a short circuit for AC and contributes stability for DC quiescent condition. Hence capacitor is connected in parallel with emitter resistance.

$$X_{CE} \ll R_E$$

The coupling capacitor:

An amplifier amplifies the given AC signal. In order to have noiseless transmission of a signal (without DC), it is necessary to block DC i.e. the direct current should not enter the amplifier or load. This is usually accomplished by inserting a coupling capacitor between two stages.

$$X_{CE} \ll (R_i h_{ie})$$

Frequency response :

The plot of gain versus frequency is called as frequency response.

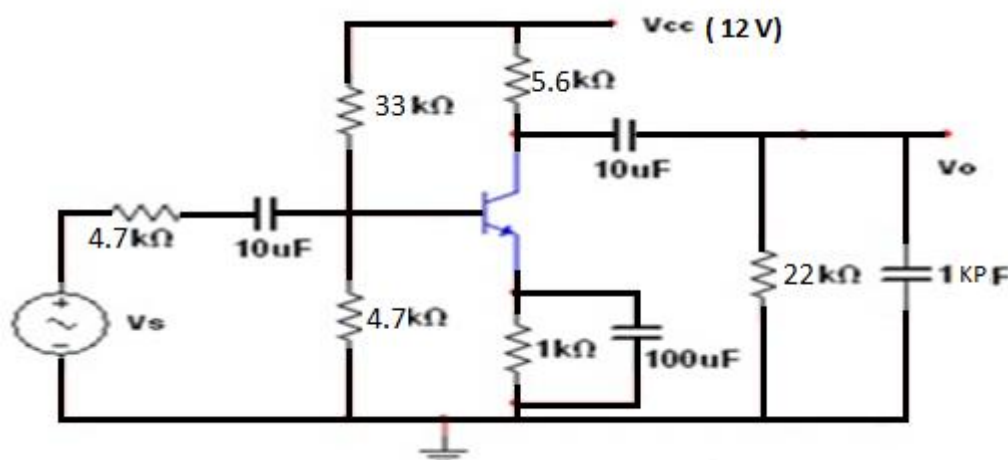
The coupling and bypass capacitors causes the gain to fall at low frequency region and internal parasitic capacitance and shunt capacitor causes the gain to fall at high frequency region.

In the mid frequency range large capacitors are effectively short circuits and the stray capacitors are open circuits, so that no capacitance appear in the mid frequency range. Hence the mid band frequency gain is maximum.

Characteristics of CE Amplifier:

1. Large current gain.
2. Large voltage gain.
3. Large power gain.
4. Current and voltage phase shift of 180° .
5. Moderated output resistance.

Type	A_i	R_i	A_v	R_o
CE	$-h_{fe}$	h_{ie}	$-h_{fe} \frac{R'_L}{h_{ie}}$	∞

Circuit Diagram:

Fig(1).RC Coupled CE BJT Amplifier

Procedure:

1. Connect the circuit as shown in the circuit diagram.
2. Set source voltage = 50mV (say) at 1 KHz frequency using the function generator.
3. Keeping input voltage constant vary the frequency from 50 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: gain (dB) versus Frequency on a semi log graph sheet.
5. Calculate the bandwidth from the graph.

Observations:.

$$V_S = 50\text{mV}$$

DC conditions:-

$$V_{BE} = \dots\dots\dots$$

$$V_{CE} = \dots\dots\dots$$

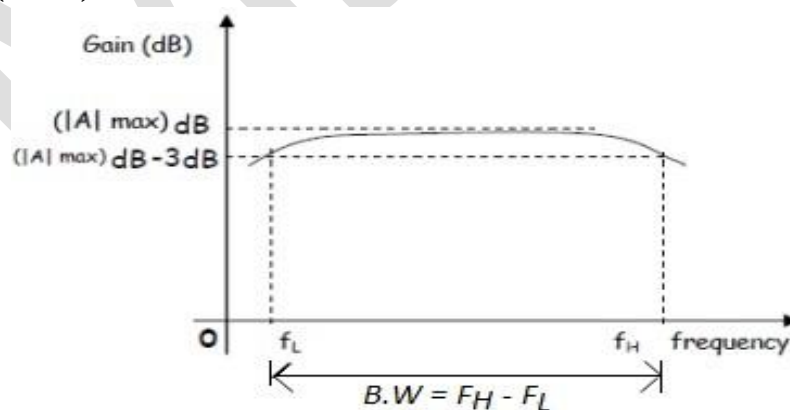
$$I_B = \dots\dots\dots$$

$$I_C = \dots\dots\dots$$

Frequency	Vo(Volts)	Gain = Vo/Vs	Gain(dB) = 20 log(Vo/Vs)

Graph:

In the usual application, mid band frequency range are defined as those frequencies at which the response has fallen to 3dB below the maximum gain ($|A|_{\text{max}}$). These are shown as f_L and f_H and are called as the 3dB frequencies are simply the lower and higher cut off frequencies respectively. The difference between higher cut off and lower cut off frequency is referred to as bandwidth ($f_H - f_L$).



Fig(2).Frequency Response Curve Of RC coupled BJT CE Amplifier

Precautions:

1. While performing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.
2. Connect signal generator in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base and collector terminals of the transistor.

Result:

1. The BJT CE amplifier is studied
2. The frequency response curve of the BJT CE amplifier is plotted.
3. Lower cutoff frequency, $f_L = \dots\dots\dots$
Higher cutoff frequency, $f_H = \dots\dots\dots$
Bandwidth = $f_H - f_L = \dots\dots\dots$

Viva Questions:**1. What is the equation for voltage gain?****Ans:**

$$A_V = -h_{fe} \frac{R'_L}{h_{ie}}$$

2. What is cut off frequency?

Ans: In electronics, cutoff frequency or corner frequency is the frequency either above or below which the power output of a circuit, such as a line, amplifier, or electronic filter has fallen to a given proportion of the power in the pass band. Most frequently this proportion is one half the pass band power, also referred to as the 3 dB point since a fall of 3 dB corresponds approximately to half power. As a voltage ratio this is a fall to $\frac{1}{\sqrt{2}}$ of the pass band voltage

3. What are the applications of CE amplifier?

Ans: Low frequency voltage amplifier, radio frequency circuits and low-noise amplifiers

4. What is active region?

Ans: The active region of a transistor is when the transistor has sufficient base current to turn the transistor on and for a larger current to flow from emitter to collector. This is the region where the transistor is on and fully operating. In this region JE in forward bias and JC in reverse bias and transistor works as an amplifier

5. What is Bandwidth?

Ans: Bandwidth is the difference between the upper and lower frequencies in a continuous set of frequencies. It is typically measured in hertz, and may sometimes refer to passband bandwidth, sometimes to baseband bandwidth, depending on context. Passband bandwidth is the difference between the upper and lower cutoff frequencies of, for example, a bandpass filter, a communication channel, or a signal spectrum. In case of a low-pass filter or baseband signal, the bandwidth is equal to its upper cutoff frequency.

Experiment No: 10

Common Source JFET Amplifier

Aim:

1. To plot the frequency response of a JFET common source amplifier .
2. To find the input and output impedances of the CS amplifier
3. To find the cut off frequencies, Bandwidth and calculate its gain.

Components:

Name	Quantity
JFET BFW 11	1
Resistor $6.8K\Omega$, $8.2K\Omega$, $1M\Omega$	2, 1, 1
Capacitor $10\mu F$, $100\mu F$	2,1

Equipment:

Name	Range	Quantity
Bread Board		1
Dual power supply	0-30V	1
CRO	(0-20)MHz	1
Function Generator	(0-1)MHz	1
Connecting Wires		

Specifications:**For FET BFW11:**

Gate Source Voltage $V_{GS} = -30V$

Forward Gain Current $I_{GF} = 10mA$

Maximum Power Dissipation $P_D = 300mW$

Theory:

Of the possible three configurations of JFET amplifiers, common source (CS) configuration is mostly used. The advantage of using CS configuration is that it has very high input impedance.

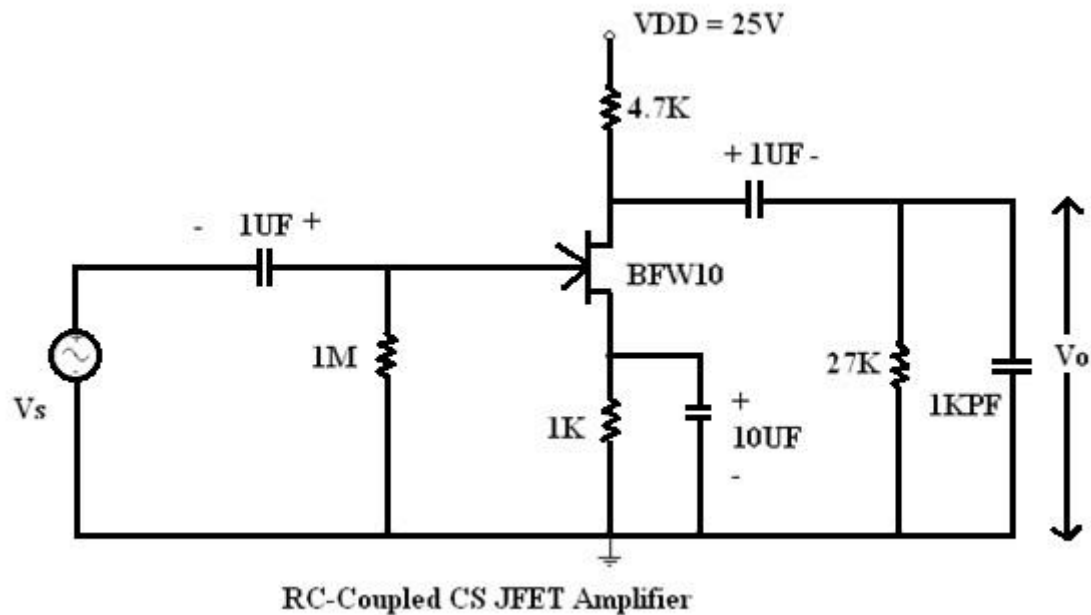
Circuit diagram shows the FET amplifier of common source configuration. The biasing input and couplings are shown in the figure. The mid range voltage gain of the amplifier is given by $A = g_m(r_d \parallel R_L)$

At the mid-frequency range, there is no effect of input and output coupling capacitors. Therefore, the voltage gain and phase angle are constant in this frequency range. The amplifier shown in the circuit diagram has only two RC networks that influence its low-frequency response. One network is formed by the output coupling capacitors and the output impedance looking at the drain. Just as in the case of BJT amplifier, the reactance of the input coupling capacitor, reactance increases as the frequency decreases. The phase angle also changes with change in frequency.

As the frequency is increased beyond mid-frequency range the internal transistor capacitance effect is predominant. For JFET's C_{gs} is the internal capacitance between gate and source. This is also called input capacitance, C_{gs} . The other internal capacitance, which effects the

performance is acts as a feedback circuit, which couples both, input and output. The effect of both these capacitances is that it reduced the gain appreciably as in the case of BJT.

Circuit Diagram:



Fig(1)- RC Coupled CS JFET Amplifier

Procedure:

1. Connect the circuit as shown in the circuit diagram.
2. Set source voltage $V_s = 50\text{mV}$ (say) at 1 KHz frequency using the function generator.
3. Keeping input voltage constant vary the frequency from 50 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: gain (dB) verses Frequency on a semi log graph sheet.
5. Calculate the bandwidth from the graph.
6. Calculate all the parameters at mid band frequencies (i.e. at 1 KHz).
7. To calculate voltage gain

$$\text{Gain } A_{VS} = \text{Output Voltage } (V_o) / \text{Source Voltage } (V_s)$$

Observations:

DC conditions:-

$$V_{GS} = \dots\dots\dots$$

$$V_{DS} = \dots\dots\dots$$

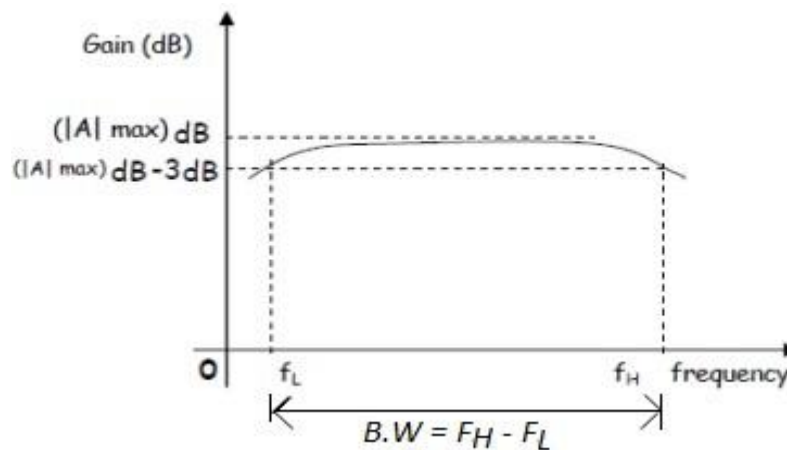
$$I_D = \dots\dots\dots$$

$$V_s = 50\text{mV}$$

Frequency	Vo(volts)	Gain= Vo/Vs	Gain(dB)=20 log(Vo/Vs)

Graph:

In the usual application, mid band frequency range are defined as those frequencies at which the response has fallen to 3dB below the maximum gain ($|A|_{\max}$). These are shown as f_L and f_H and are called as the 3dB frequencies are simply the lower and higher cut off frequencies respectively. The difference between higher cut off and lower cut off frequency is referred to as bandwidth ($f_H - f_L$).



Fig(2)-.Frequency Response Curve Of RC coupled CS JFET Amplifier

Precautions:

1. While performing the experiment do not exceed the ratings of the FET. This may lead to damage the FET.
2. Connect voltmeter and ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the Source, Drain and Gate terminals of the transistor

Result:

1. The JFET CS amplifier is studied
2. The frequency response curve of the JFET CS amplifier is plotted.
3. The cut off frequencies and Bandwidth is found
 Lower cutoff frequency, $f_L = \dots\dots\dots$
 Higher cutoff frequency, $f_H = \dots\dots\dots$
 Bandwidth = $f_H - f_L = \dots\dots\dots$

Viva Questions:**1. Why FET is called as unipolar device?**

Ans: FETs are unipolar transistors as they involve single-carrier-type operation.

2. Why the common-source (CS) amplifier may be viewed as a transconductance amplifier or as a voltage amplifier?

Ans: As a transconductance amplifier, the input voltage is seen as modulating the current going to the load. As a voltage amplifier, input voltage modulates the amount of current

flowing through the FET, changing the voltage across the output resistance according to Ohm's law. However, the FET device's output resistance typically is not high enough for a reasonable transconductance amplifier (ideally infinite), nor low enough for a decent voltage amplifier (ideally zero).

3. What are the characteristics of JFET source amplifier?

Ans: At low frequencies and using a simplified [hybrid-pi model](#), the following [small-signal](#) characteristics can be derived.

	Definition	Expression
Current Gain	$A_i \triangleq \frac{i_{out}}{i_{in}}$	∞
Input Impedance	$r_{in} \triangleq \frac{v_{in}}{i_{in}}$	∞
Voltage Impedance	$A_v \triangleq \frac{v_{out}}{v_{in}}$	$-g_m R'_L$
Output Impedance	$r_{out} \triangleq \frac{v_{out}}{i_{out}}$	R_D

4. What is the impedance of FET?

Ans: $r_{in} \triangleq \frac{v_{in}}{i_{in}}$

Experiment No:11**UJT Characteristics and Silicon-Controlled Rectifier (SCR) Characteristics****Aim:**

- 1) To study the static characteristics of a given UJT (2N2646)
- 2) Identify the negative resistance region and estimate the resistance of the device.
- 3) To draw the V-I Characteristics of Silicon controlled rectifier.

Components:

Name	Quantity
UJT 2N 2646	1
Resistor 1 K?	2
SCR (TYN616)	1
Resistors 10k Ω , 1k Ω	1

Equipment:

Name	Range	Quantity
Bread Board		1
Dual power supply	0-30V	1
Digital Ammeter	(0-200)mA	1
Digital Voltmeter	(0-20)V	1
Connecting Wires		

Specifications:**UJT 2N- 2646:**Peak emitter current (I_p) = 2AContinuous emitter current (I_E) = 50mAInter Base Voltage (V_{BB}) = 35VEmitter Base Reverse Voltage (V_{EB2}) = -30V

Power dissipation at 25° C= 300mW

SCR TYN616

IGT= 25mA

VGT = 1.3 V

IH = 40 mA

IL = 60 mA

dV/dt = 500 V/ μ s

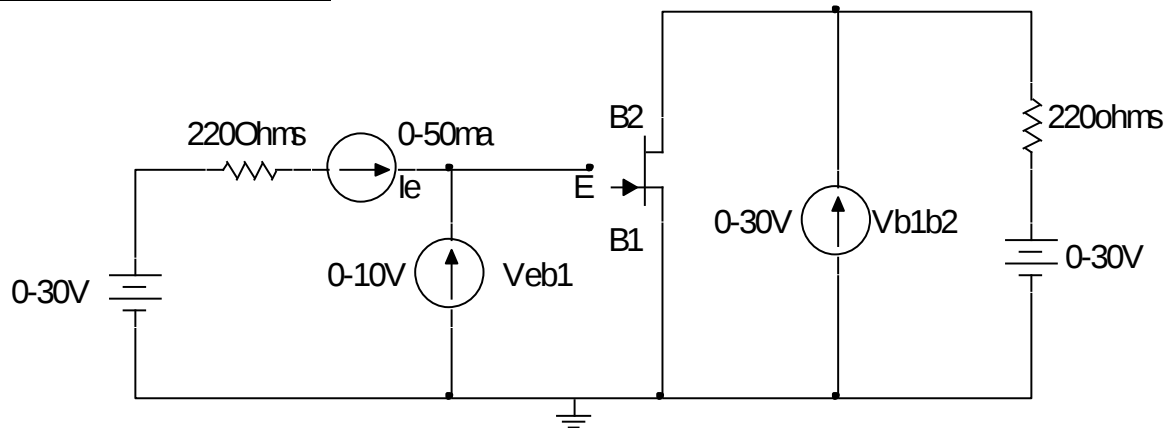
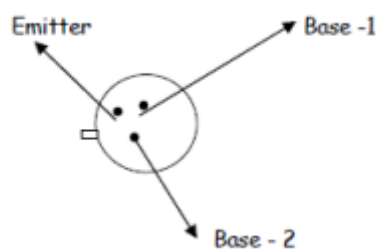
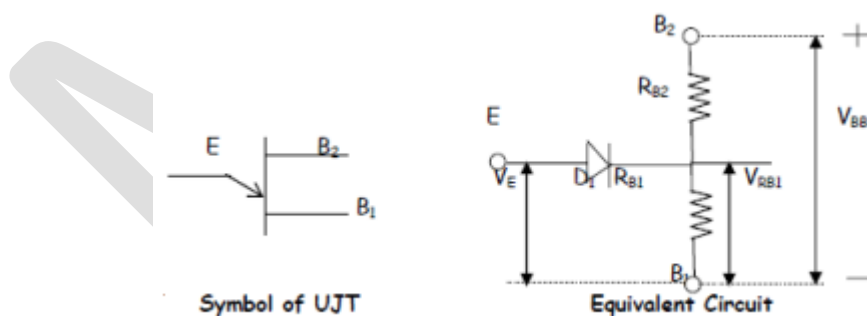
Circuit Diagram of UJT:

Fig.1

Figure 1: Circuit Diagram of Unijunction transistor characteristics

Pin assignment of UJT:

Theory: The UJT- junction is a 3-terminal solid-state device (emitter and the two bases). The simplified equivalent circuit is shown below:



The device has only one PN junction and hence it is known as UNI-JUNCTION transistor. The PN junction is formed between the emitter and the base regions. The emitter region is heavily doped. The PN emitter to base junction is shown as diode D1. The emitter region is closer to base (B1) terminal than base (B2). The inter base resistance of the N-type Si bar appears as two resistors. The operational difference between FET and UJT is that FET is normally operated with gate junction reverse biased, whereas useful behavior of UJT occurs when the emitter is forward biased.

The emitter conductivity characteristics are such that as increases the emitter to base (B1) voltage decreases. At a peak point and the valley point, the slope of the emitter

characteristics is 0. At points to the left of to E-B1 is forward biased and exists. Between and increase in is accompanied by a relation in emitter voltage . This is the negative resistance region of UJT. Beyond the valley point an increase in is accomplished by an increase in . This region is known as the saturation region.

Procedure:

1. Connect the circuit as shown in the figure 1
2. Ensure that the power supply is switched OFF. Keep the voltage control knob in the minimum position and current control knob in maximum position.
3. Switch ON the power supply Keep V_{BB} at 5volts. Now vary V_{EB1} by varying VEE. Note down I_E once UJT is ON, Increase the emitter current I_E in small steps of 5mA and note down the corresponding V_{EB1} value upto a maximum of 50mA.
4. Repeat above steps for $V_{BB} = 8V$. Plot graph of I_E versus V_{EB1} for different values of V_{BB} .
5. Calculate resistance of the UJT in the negative resistance region using the formula

$$r(-) = \frac{\Delta V_{EB1}}{\Delta I_E} \quad \text{at } V_{BB} = \text{Constant}$$

Observations:

$V_{BB} = 5V$		$V_{BB} = 8V$	
$I_E(\text{mA})$	$V_{EB1}(\text{V})$	$I_E(\text{mA})$	$V_{EB1}(\text{V})$

Expected graph:

Plot the tabulated readings on a graph sheet with on X-axis and on Y-axis.

Inference:

1. There is a negative resistance region from peak point to valley point.
2. Increase in increases the value of peak and valley voltages.

Precautions:

1. While performing the experiment do not exceed the ratings of the UJT. This may lead to damage of the UJT.
2. Connect voltmeter and ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base-1, base-2 terminals of UJT.

Result:

The emitter characteristics of UJT have been determined.

Viva questions:**1. Write the features of UJT.**

Ans: The device has only one junction, so it is called the uni-junction device. The device, because of one P-N junction, is quite similar to a diode but it differs from an ordinary diode as it has three terminals.

In a uni-junction transistor the emitter is heavily doped while the N-region is lightly doped, so the resistance between the base terminals is relatively high, typically 4 to 10 kilo Ohm when the emitter is open. The N-type silicon bar has a high resistance and the resistance between emitter and base-1 is larger than that between emitter and base-2. It is because emitter is closer to base-2 than base-1. UJT is operated with emitter junction forward-biased while the JFET is normally operated with the gate junction reverse-biased. UJT does not have ability to amplify but it has the ability to control a large ac power with a small signal. It exhibits a negative resistance characteristic and so it can be employed as an oscillator.

2. What is the difference between UJT and FET?

Ans: The structure of a UJT is quite similar to that of an N-channel JFET. The main difference is that P-type (gate) material surrounds the N-type (channel) material in case of JFET and the gate surface of the JFET is much larger than emitter junction of UJT.

3. What is a UJT?

Ans: It is Uni-junction transistor, it has only one junction between emitter and n-slab.

4. What is relaxation oscillator?

Ans: A relaxation oscillator is an oscillator based upon the behavior of a physical system's return to equilibrium after being disturbed. That is, a dynamical system within the oscillator continuously dissipates its internal energy. Normally the system would return to its natural equilibrium; however, each time the system reaches some threshold sufficiently close to its equilibrium, a mechanism disturbs it with additional energy. Hence, the oscillator's behavior is characterized by long periods of dissipation followed by short impulses. The period of the oscillations is set by the time it takes for the system to relax from each disturbed state to the threshold that triggers the next disturbance.

5. Application of UJT?

Ans: Relaxation oscillator, Saw tooth wave form generator

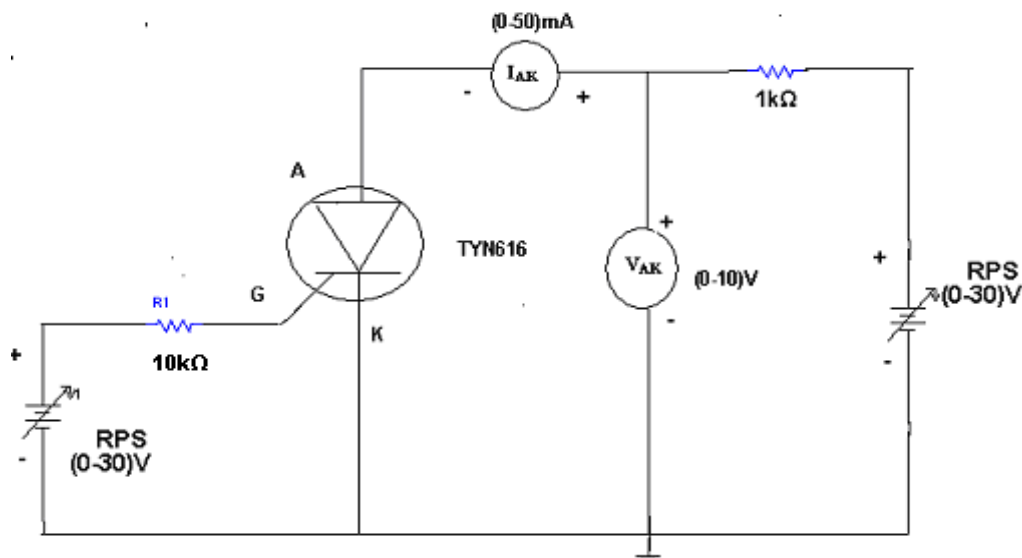
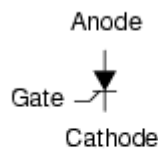
Circuit Diagram of SCR:

Figure 2: Circuit Diagram of SCR characteristics

Theory:

It is a four layer semiconductor device being alternate of P-type and N-type silicon. It consists of 3 junctions J_1 , J_2 , J_3 the J_1 and J_3 operate in forward direction and J_2 operates in reverse direction and three terminals called anode A, cathode K, and a gate G. The operation of SCR can be studied when the gate is open and when the gate is positive with respect to cathode.

*Schematic symbol*

When gate is open, no voltage is applied at the gate due to reverse bias of the junction J_2 no current flows through R_2 and hence SCR is at cutt off. When anode voltage is increased J_2 tends to breakdown.

When the gate positive, with respect to cathode J_3 junction is forward biased and J_2 is reverse biased. Electrons from N-type material move across junction J_3 towards gate while holes from P-type material moves across junction J_3 towards cathode. So gate current starts flowing, anode current increase is in extremely small current junction J_2 break down and SCR conducts heavily.

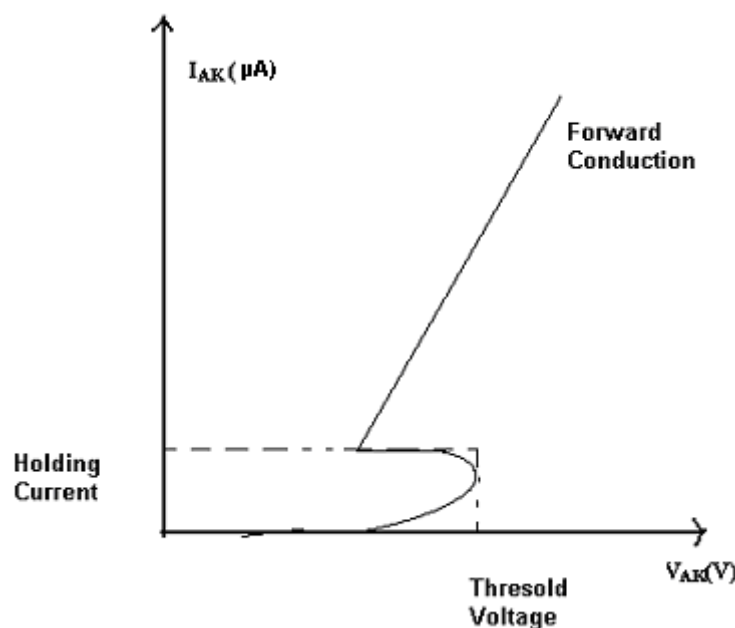
When gate is open the breakover voltage is determined on the minimum forward voltage at which SCR conducts heavily. Now most of the supply voltage appears across the load resistance. The holding current is the maximum anode current gate being open, when break over occurs.

Procedure:

1. Connections are made as per figure 2.
2. Keep the gate supply voltage at some constant value
3. Vary the anode to cathode supply voltage and note down the readings of voltmeter and ammeter. Keep the gate voltage at standard value.
4. A graph is drawn between V_{AK} and I_{AK} .

Observation:

$V_{AK}(V)$	$I_{AK} (\mu A)$

Model Wave form:

Result: SCR Characteristics are observed.

Viva questions:**1. What is an SCR?**

Ans: Silicon-controlled rectifier (or semiconductor-controlled rectifier) is a four-layer solid state current controlling device. The name "silicon controlled rectifier" or SCR is General Electric's trade name for a type of thyristor

2. What is the difference between SCR and TRIAC?

Ans: SCRs are unidirectional devices (i.e. can conduct current only in one direction) as opposed to TRIACs which are bidirectional (i.e. current can flow through them in either direction). SCRs can be triggered normally only by currents going into the gate as opposed to

TRIACs which can be triggered normally by either a positive or a negative current applied to its gate electrode.

3. What are the applications of SCR?

Ans: SCRs are mainly used in devices where the control of high power, possibly coupled with high voltage, is demanded. Their operation makes them suitable for use in medium to high-voltage AC power control applications, such as lamp dimming, regulators and motor control.

SCRs and similar devices are used for rectification of high power AC in high-voltage direct current power transmission. They are also used in the control of welding machines, mainly MTAW and GTAW processes.

4. Why is Peak Reverse Voltage Important?

Ans: When an SCR is used for rectification, during the negative half cycle of given ac supply, reverse voltage is applied across the SCR. If Peak Reverse Voltage is exceeded, there may be an avalanche breakdown and the SCR will be damaged (unless the external circuit limits the current). Commercial SCRs have a PRV up to 2.5kV.

5. What is asymmetrical SCR?

Ans: SCR incapable of blocking reverse voltage are known as asymmetrical SCR, abbreviated ASCR. They typically have a reverse breakdown rating in the 10's of volts. ASCR are used where either a reverse conducting diode is applied in parallel (for example, in voltage source inverters) or where reverse voltage would never occur (for example, in switching power supplies or DC traction choppers).

Asymmetrical SCR can be fabricated with a reverse conducting diode in the same package. These are known as RCT, for reverse conducting thyristor

APPENDIX

LABORATORY COURSE ASSESSMENT GUIDELINES

- i. The number of experiments in each laboratory course shall be as per the curriculum in the scheme of instructions provided by OU. Mostly the number of experiments is 10 in each laboratory course under semester scheme and 18 under year wise scheme.
- ii. The students will maintain a separate note book for observations in each laboratory course.
- iii. In each session the students will conduct the allotted experiment and enter the data in the observation table.
- iv. The students will then complete the calculations and obtain the results. The course coordinator will certify the result in the same session.
- v. The students will submit the record in the next class. The evaluation will be continuous and not cycle-wise or at semester end.
- vi. The internal marks of 25 are awarded in the following manner:
 - a. Laboratory record - Maximum Marks 15
 - b. Test and Viva Voce - Maximum Marks 10
- vii. Laboratory Record: Each experimental record is evaluated for a score of 50.
The rubric parameters are as follows:
 - a. Write up format - Maximum Score 15
 - b. Experimentation Observations & Calculations - Maximum Score 20
 - c. Results and Graphs - Maximum Score 10
 - d. Discussion of results - Maximum Score 5

While (a), (c) and (d) are assessed at the time of record submission, (b) is assessed during the session based on the observations and calculations. Hence if a student is absent for an experiment but completes it in another session and subsequently submits the record, it shall be evaluated for a score of 30 and not 50.

- viii. The experiment evaluation rubric is therefore as follows:

Parameter	Max Score	Outstanding	Accomplished	Developing	Beginner	Points
Observations and Calculations	20					
Write up format	15					
Results and graphs	10					
Discussion of Results	5					

LABORATORY EXPERIMENT EVALUATION RUBRIC

CATEGORY	OUTSTANDING (Up to 100%)	ACCOMPLISHED (Up to 75%)	DEVELOPING (Up to 50%)	BEGINNER (Up to 25%)
Write up format	Aim, Apparatus, material requirement, theoretical basis, procedure of experiment, sketch of the experimental setup etc. is demarcated and presented in clearly labeled and neatly organized sections.	The write up follows the specified format but a couple of the specified parameters are missing.	The report follows the specified format but a few of the formats are missing and the experimental sketch is not included in the report	The write up does not follow the specified format and the presentation is shabby.
Observations and Calculations	The experimental observations and calculations are recorded in neatly prepared table with correct units and significant figures. One sample calculation is explained by substitution of values	The experimental observations and calculations are recorded in neatly prepared table with correct units and significant figures but sample calculation is not shown	The experimental observations and calculations are recorded neatly but correct units and significant figures are not used. Sample calculation is also not shown	The experimental observations and results are recorded carelessly. Correct units significant figures are not followed and sample calculations not shown
Results and Graphs	Results obtained are correct within reasonable limits. Graphs are drawn neatly with labeling of the axes. Relevant calculations are performed from the graphs. Equations are obtained by regression analysis or curve fitting if relevant	Results obtained are correct within reasonable limits. Graphs are drawn neatly with labeling of the axes. Relevant calculations from the graphs are incomplete and equations are not obtained by regression analysis or curve fitting	Results obtained are correct within reasonable limits. Graphs are not drawn neatly and or labeling is not proper. No calculations are done from the graphs and equations are not obtained by regression analysis or curve fitting	Results obtained are not correct within reasonable limits. Graphs are not drawn neatly and or labeling is not proper. No calculations are done from the graphs and equations are not obtained by regression analysis or curve fitting
Discussion of results	All relevant points of the result are discussed and justified in light of theoretical expectations. Reasons for divergent results are identified and corrective measures discussed.	Results are discussed but no theoretical reference is mentioned. Divergent results are identified but no satisfactory reasoning is given for the same.	Discussion of results is incomplete and divergent results are not identified.	Neither relevant points of the results are discussed nor divergent results identified

ix. The first page of the record will contain the following title sheet:

SAMPLE ASSESSMENT SHEET**NAME:****ROLL NO.**

Exp. No.	Date conducted	Date Submitted	Observations & Calculations (Max 20)	Write up (Max 15)	Results and Graphs (Max 10)	Discussion of Results (Max 5)	Total Score (Max 50)
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							

- x. The 15 marks of laboratory record will be scaled down from the TOTAL of the assessment sheet.
- xi. The test and viva voce will be scored for 10 marks as follows:

Internal Test	-	6 marks
Viva Voce / Quiz	-	4 marks
- xii. Each laboratory course shall have 5 course outcomes.

The proposed course outcomes are as follows:

On successful completion of the course, the student will acquire the ability to:

1. Conduct experiments, take measurements and analyze the data through hands-on experience in order to demonstrate understanding of the theoretical concepts of _____, while working in small groups.
 2. Demonstrate writing skills through clear laboratory reports.
 3. Employ graphics packages for drawing of graphs and use computational software for statistical analysis of data.
 4. Compare the experimental results with those introduced in lecture, draw relevant conclusions and substantiate them satisfactorily.
 5. Transfer group experience to individual performance of experiments and demonstrate effective oral communication skills.
- xiii. The Course coordinators would prepare the assessment matrix in accordance with the guidelines provided above for the five course outcomes. The scores to be entered against each of the course outcome would be the sum of the following as obtained from the assessment sheet in the record:
- a. Course Outcome 1: Sum of the scores under 'Observations and Calculations'.
 - b. Course Outcome 2: Sum of the scores under 'Write up'.
 - c. Course Outcome 3: Sum of the scores under 'Results and Graphs'.
 - d. Course Outcome 4: Sum of the scores under 'Discussion of Results'.
 - e. Course Outcome 5: Marks for 'Internal Test and Viva voce'.
- xiv. Soft copy of the assessment matrix would be provided to the course coordinators.

MUFFAKHAM JAH COLLEGE OF ENGINEERING AND TECHNOLOGY**Program Outcomes of B.E (ECE) Program:**

PO1: Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: Problem analysis: Identify, formulate, research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences

PO3: Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal, and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO 12: Life-long learning: Recognise the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs) of ECE Department, MJCET

PSO1: The ECE Graduates will acquire state of art analysis and design skills in the areas of digital and analog VLSI Design using modern CAD tools.

PSO2: The ECE Graduates will develop preliminary skills and capabilities necessary for embedded system design and demonstrate understanding of its societal impact.

PSO3: The ECE Graduates will obtain the knowledge of the working principles of modern communication systems and be able to develop simulation models of components of a communication system.

PSO4: The ECE Graduates will develop soft skills, aptitude and programming skills to be employable in IT sector.